A Novel Improved Soft Switching PWM DC-DC Converter

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Abstract: A new zero-voltage switching (ZVS) pulse width modulation (PWM) DC-DC converter using MOSFETs is proposed in this paper. The proposed converter achieves ZVS with reduction in voltage and current stresses across switches to improve the efficiency by minimizing the switching and conduction losses. The predicted operation principles and theoretical analysis of the presented converter are verified with a prototype of a 360 W, 50 V/6 V and 100 kHz PWM half bridge buck converter. Additionally, at full output power in the proposed soft switching converter the overall efficiency, which is 80% in the hard switching case, increases to about 95%.

Keywords: PWM, DC-DC converter, ZVS.

I. INTRODUCTION

With advance in VLSI technology, smaller, more powerful digital system is available. It requires power supply with higher power density, lower profile and higher efficiency. To further increase the processing speed and efficiency, operating voltage is continuously reduced. With advance in VLSI technology, smaller, more powerful digital system is available. It requires power supply with higher power density, lower profile and higher efficiency. To further increase the processing speed and efficiency, operating voltage is continuously reduced with increase in operating current. Also fast transient response and smaller size for a given power supply becomes very important [1][2]. PWM topologies have been widely used for this application. Unfortunately, hold up time requirement put huge penalties on the performance of these topologies. Also, high switching loss limited the power density achievable for these topologies. Excessive switching loss prohibited higher switching frequency. Soft switching converters employing two transformers have been researched in recent years for power converters to reduce switching losses [3]. High frequency PWM DC-DC converters have been widely used in industry due to their high power density, fast response and control simplicity [4]. Especially at high frequencies and high power levels, it is necessary to use advanced soft switching techniques to reduce switching losses. In this paper, a simple and new topology is introduced to achieve higher efficiency as compared to the conventional converter. This proposed converter utilizes three clamped capacitors in the primary side of the transformer to provide low output voltage. The capacitor used in series with the transformer provides better dead time control. The resonance between two capacitors in arm of the bridge and the leakage inductance of the transformer make the switches turned on/off under zero voltage switching (ZVS). It's simple configuration, make easy to control. With less number of components, this converter becomes more economical and attractive as compared to other previously researched converter. In the reference papers, different soft switching techniques are used to reduce switching losses and the operations are analysed properly. But the duration of current flowing through the body diode of MOSFET switches is not controlled in past work.

In the reference papers, different soft switching techniques are used to reduce switching losses and the operations are analysed properly. But the duration of current flowing through the body diode of MOSFET switches is not controlled in past work. During transition periods, high input current may flow through the switches, in result conduction losses may occur. This problem can be avoided by using an inductor in series with the supply.

This proposed converter is designed to solve the above problems. The following points have to follow in the paper:

- description of topology used and design process
- design of blocking capacitor for dead time control
- design of transformer leakage inductance so that the stored energy should transfer properly to supply during off time.

II. OPERATION PRINCIPLES AND ANALYSIS

The following assumptions are made to simplify the circuit operations

- secondary side leakage inductance is neglected;
The capacitance of the blocking capacitor is taken more as compared to other two capacitors used in this circuit; capacitances of other two capacitors are taken as same value; turn ratio of transformer is taken asymmetrical; to make magnetizing current ripple free, magnetizing inductance \( L_m \) is chosen as high value; current flowing through transformer is continuous.

The proposed converter scheme is shown in Fig.1. The circuit scheme includes two MOSFET switches \( Q_1 \) and \( Q_2 \). Two clamp capacitors \( C_1 \) and \( C_2 \). The transformer \( T_x \) denotes the combination of the magnetizing inductance \( L_m \), the leakage inductance \( L_k \) and the ideal transformer with transformer winding-ratio \( n:1 \). The proposed dc-dc converter is designed through AC link as energy transfer devices. In steady-state, the proposed converter has four operation states during one switching cycle. The key waveforms and the equivalent circuits of each operation state are shown in Fig.2 and Fig.3, respectively.

**Mode 1 ( \( t_0-t_1 \) )**:
At \( t = t_0 \), MOSFET \( Q_1 \) is turned on by providing proper gate pulse. Now current starts to flow through the transformer. With the induction property, the diode \( D_2 \) is compelled to conduct. Resonant condition occurs by the magnetizing inductance \( L_m \) and equivalent capacitance of \( C_b \) and \( C_1 \). But the resonant period is less, so high peak current and voltage stresses cannot appear across the switch \( Q_1 \).

The voltage and current expression will be as

\[
i_L(t-t_0) = \frac{V}{L} \left[ \frac{P \sin \sqrt{k_1} (t-t_0) + Q \sin \sqrt{k_2} (t-t_0)}{\sqrt{k_1}} \right]
\]

\[
u_{C_1}(t-t_0) = \frac{V}{L C_1} \left[ \frac{P}{\sqrt{k_1}} \cos \sqrt{k_1} (t-t_0) \right]
\]

\[
u_{C_2}(t-t_0) = \frac{V}{L C_2} \left[ \frac{Q}{\sqrt{k_2}} \cos \sqrt{k_2} (t-t_0) \right]
\]

Where \( P, Q, k_1 \) and \( k_2 \) are function of \( L, L_p, C_1, C_2, C_b \), which is a big expression.

The switch is turned on under ZVS due to capacitor \( C_1 \), and turned off under ZCS due to transformer leakage inductance \( L_p \). This mode is ended when capacitor \( C_1 \) completely discharge its energy to capacitor \( C_b \) and \( L_1 \). At this moment input current completely flow through capacitor \( C_1 \), providing current through the switch equal to zero. So at this moment switch \( Q_1 \) can be turned off under ZCS. At end of this mode, \( C_b \) charged up to \( C_{b1} \) opposite to that of its initial value.

At \( t = t_1 \), \( i_l(t_1) = I_{L1} \), \( V_{C1} = 0 \), \( V_{Cb} = V_{Cb1} \), \( V_{C2} = V_{C2} \).

**Mode 2 ( \( t_1-t_2 \) )**:
At \( t = t_1 \), stored energy of inductor is forced the body diode of switch to conduct and inductor discharged its stored energy through \( C_2-Dq_2-Cb \). Resonance occur between leakage inductance \( L_p \) and capacitors \( C_2 \) and \( C_b \). However, the resonant period is not more than the dead time. Dead time is controlled by capacitor \( C_b \). This mode ends at \( t_2 \), when current through \( C_b \) becomes zero i.e. this blocking capacitor is charged upto its maximum value.

The voltage and current expressions for this mode are given below.

![Fig. 2. Key waveforms of the proposed converter](image-url)
Fig. 3

Modes of Operation

$$i_L(t-t_1) = \frac{V-v_{C2}'}{L} \left[ R \sin \sqrt{k_3} (t-t_1) + S \sin \sqrt{k_4} (t-t_1) \right] + I_{L1} \left[ R \cos \sqrt{k_3} (t-t_1) + S \cos \sqrt{k_4} (t-t_1) \right]$$

(4)

$$i_{LP}(t-t_1) = I_{L1} \cos \frac{1}{\sqrt{L_pC_p}}(t-t_1)$$

$$-\frac{v_{C2}'}{Z_1} + v_{C2} \sin \frac{1}{\sqrt{L_pC_p}}(t-t_1)$$

(5)

$$v_{Cb}(t-t_1) = I_{L1} \sqrt{\frac{L_pC_p}{C_b}} \sin \frac{1}{\sqrt{L_pC_p}}(t-t_1) + \left( v_{C2} + v_{C1} \right) C_p \cos \frac{1}{\sqrt{L_pC_p}}(t-t_1)$$

(6)

Now the voltage across capacitor $C_2$ can be expressed as

$$v_{C2}(t-t_1) = \frac{V-v_{C2}'}{LC_2} \left[ -\frac{R \cos \sqrt{k_3} (t-t_1)}{\sqrt{k_3}} - \frac{S \cos \sqrt{k_4} (t-t_1)}{\sqrt{k_4}} \right] + \frac{I_{L1}}{C_2} \left[ R \sin \sqrt{k_3} (t-t_1) + S \sin \sqrt{k_4} (t-t_1) \right]$$

(7)

Mode 3 (t2-t3) : This mode starts with switch Q2 turned on under ZVS, diode D1 on with D2 off. This mode will come to end with capacitor $C_b$ charged up to peak value, but with opposite polarity as compared to previous mode. This mode is ended when capacitor $C_2$ completely discharge its energy to capacitor $C_b$ and $L_p$. At this moment input current completely
flow through capacitor C2, providing current through the switch Q2 equal to zero. So at this moment switch Q2 can be
turned off under ZCS. At end of this mode, Cb charged up to
Cb2 opposite to that of its initial value.
The voltage and current expression for this mode is given as follows,
\[ i_k(t-t_2) = I_{L2}\left[ T \cos \sqrt{k_5}(t-t_2) + U \cos \sqrt{k_6}(t-t_2) \right] + \left( \frac{V - v_e}{L} + \frac{v_{c2}}{L} \right) \left[ T \sin \sqrt{k_5}(t-t_2) + U \sin \sqrt{k_6}(t-t_2) \right] \]

At the end of this mode, current through transformer is zero.
\[ v_{c2}(t-t_2) = I_{L2}\left[ T \sin \sqrt{k_5}(t-t_2) + U \sin \sqrt{k_6}(t-t_2) \right] + \left( \frac{V - v_e}{L} + \frac{v_{c2}}{L} \right) \left[ T \cos \sqrt{k_5}(t-t_2) + U \cos \sqrt{k_6}(t-t_2) \right] \]

Mode 4 (t3-t4) : The transformer start to transfer stored energy to secondary side as well as to capacitor C1, which
ensure the continuous flow of current at the output. Then the
rectified diode D2 will start to conduct, while diode D1 will be
turned off under ZVS. The body diode of the switch Q1 is
turned on due to the energy transferring property of inductor in
the same direction in which it get charged. The mode ends at
t4, when current through Cb becomes zero i.e. this blocking
capacitor is charged up to its maximum value.
The voltage and current expression for this mode is given as follow:
\[ i_{Lp}(t-t_3) = I_{Lp}\cos \frac{1}{\sqrt{L_p C_e}}(t-t_3) \]
\[ i_L(t-t_3) = \frac{V}{Z_3} \sin \frac{1}{\sqrt{L_p C_e}}(t-t_3) \]
\[ + \frac{v_{cb2}}{Z_2} \sin \frac{1}{\sqrt{L_p C_e}}(t-t_3) \]
\[ \frac{v_{cb2}}{Z_2} \sin \frac{1}{\sqrt{L_p C_e}}(t-t_3) \]
\[ + \frac{v_{cb2}}{Z_2} \sin \frac{1}{\sqrt{L_p C_e}}(t-t_3) \]

\[ v_{cb}(t-t_3) = \frac{I_{Lp} + \sqrt{L_p C_e}}{C_e} \sin \frac{1}{\sqrt{L_p C_e}}(t-t_3) \]
\[ - \frac{v_{cb2}}{Z_2} \sin \frac{1}{\sqrt{L_p C_e}}(t-t_3) \]

Where T, U, k5, k6 are function of L, Lp, C1, C2, Cb,
and turn-off losses can be reduced i.e.
time control can be done smoothly, so that turn-on
and turn-off losses can be reduced i.e.
\[ t_{12} \geq \frac{C_b \left( v_{cbmax} - v_{cb1} \right)}{I_{cb1}} \]

2. The transformer leakage inductance Lp should such a
value that it can discharge its energy completely to
Cb, C1, C2 and load:
\[ \frac{1}{2} L_p I^{2}_{i_{cbmax}} = \frac{1}{2} C_b v_{cb}^2 + \frac{1}{2} C_1 v_{c1}^2 + \frac{1}{2} C_2 v_{c2}^2 \]

Transformer Design:
The inducto- transformer should be designed to minimize
the leakage inductance, ac winding losses, and core losses.

When the transformer is designed to operate in
discontinuous mode the total inductance is lower than in
continuous mode, and the size of the transformer may be
smaller. But the peak currents will be at least twice the
average current, therefore ac winding losses and core losses
are the predominant factors rather than the dc losses and core
saturation. The total losses are minimized when core losses
and winding losses are approximately the same value.

-Core selection:
To reduce the core losses, ferrite-P material is usually the
preferred material for discontinuous transformers with
operating switching frequencies higher than 100Khz.
The window shape of the core should be as wide as possible to
minimize the number of layers and therefore minimize the ac
winding losses and the leakage inductance.E-type cores with
an internal air-gap are the best choice for low cost and lower
leakage inductance. Winding techniques to minimize leakage inductance, ac losses and EMI noise:
To minimize the ac losses, leakage inductance and the EMI noise, particular attention has to be paid to the design of the primary and secondary windings of the transformer.
The primary winding should be designed for less than three layers, thus minimizing the winding capacitance and the leakage inductance of the transformer. In high switching frequency applications an additional insulating layer between windings is usually used.
If the transformer has multiple secondary windings, the highest power secondary should be closest to the primary of the transformer. For high power applications, a split primary construction is typically used to reduce the leakage inductance. To avoid high ac winding losses due to the skin effect (at high frequency currents tend to flow close to the surface of the conductor), Litz wire or Foil windings are typically used. Litz wire for power applications is usually made with a few small diameter wires twisted together in a strand, and few of these strands twisted into bigger strands. Shielding tape or an additional winding between primary and secondaries is typically used to reduce the capacitive coupling of common mode noise between primary and secondary. The end of this additional winding has to be connected to ground or to the high input voltage of the transformer.

V. BASIC CONVERTER FEATURES
The features of the proposed soft switching converter are briefly summarized as follows:
1. The proposed converter is configured in a simple way.
2. It has low cost and ease to control.
3. The converter acts as a conventional PWM converter during most of the switching cycle.
4. All the switches used in this circuit are switched on and off under ZVS and ZCS.
5. The converter has higher overall efficiency and wide load range control.
6. This converter has dead time control capability.
7. Input current is ripple freed.

III. SIMULATION AND EXPERIMENTAL RESULTS
To demonstrate the validity and performance of the proposed converter was tested experimentally and was simulated. The 360 W 50 V/6 V converter is chosen for the investigations. Ro

TABLE 1

<table>
<thead>
<tr>
<th>Component</th>
<th>Value/Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET Switch, Q1</td>
<td>Ideal IRFP250N</td>
</tr>
<tr>
<td>MOSFET Switch, Q2</td>
<td>Ideal IRFP250N</td>
</tr>
<tr>
<td>Schottky Diode, D1</td>
<td>Ideal MBR60L45CTG</td>
</tr>
<tr>
<td>Schottky Diode, D2</td>
<td>Ideal MBR60L45CTG</td>
</tr>
<tr>
<td>Input Inductor, L1</td>
<td>2μH</td>
</tr>
<tr>
<td>Capacitor, C1</td>
<td>4μF</td>
</tr>
<tr>
<td>Capacitor, C2</td>
<td>4μF</td>
</tr>
<tr>
<td>Blocking Capacitor, Cb</td>
<td>6μF</td>
</tr>
<tr>
<td>Output Inductor, Lo</td>
<td>3μH</td>
</tr>
<tr>
<td>Output Capacitor, Co</td>
<td>20μF</td>
</tr>
</tbody>
</table>

VOLTS (VQ1)

-40.00 -20.00 0.00 20.00 40.00 60.00
0370.00 0375.00 0380.00 0385.00 0390.00

VOLTS (VQ2)

-40.00 -20.00 0.00 20.00 40.00 60.00
0370.00 0375.00 0380.00 0385.00 0390.00

(a)
(b)

Fig. 4(a & b) Simulated current and voltage waveforms of switch Q1 and Q2.

B. Experimental Results
The experimental result shows that the proposed converter is properly designed with ZVS for the 100 kHz under full load condition.

TABLE 2

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Name</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer</td>
<td>Core</td>
<td>RM10×1</td>
<td>mm</td>
</tr>
<tr>
<td>Inductance</td>
<td>Lm</td>
<td>5</td>
<td>μH</td>
</tr>
<tr>
<td>Trans Ratio</td>
<td>Np:Ns:Nt</td>
<td>4:1:1</td>
<td></td>
</tr>
<tr>
<td>Leakage Inductance</td>
<td>Llk</td>
<td>0.1</td>
<td>μH</td>
</tr>
</tbody>
</table>

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C. Conclusion:
The proposed converter designed has several features and advantages: high efficiency, high power density, least size due to smaller components used, cheaper and faster switching frequency of 100 kHz. It provides better efficiency by reducing switching and conduction losses.

REFERENCES


