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An Improved Multiphase converter for New Generation Microprocessr

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Abstract— **A new multi-phase PWM DC-DC converter with an auxiliary circuit to reduced switching losses across the switches, is designed, in order to solve the problem of meeting the power supply requirements of the new generation microprocessor, which requires 40-100 A current, lower voltage and better current transient response. The multi-phase topology benefits in components size reduction resulting in power density increase that allows power supply to reduce size and increase efficiency and performances. These reductions accrue from the higher effective conversion frequency with higher frequency ripple current due to the phase interleaving process of this topology. High current multiphase buck converters are finding use in computing, graphics, and telecom applications. In this paper, designed of two phases DC-DC converter of 100W, 12 V / 1 V of efficiency 97 % is discussed in detail and experimental results are presented to support the theoretical analysis.**

***Keywords*-DC-DC; Interleaving; Multiphase; PWM;**

I. INTRODUCTION

Today, a single digital IC can require 20 to 50 Amps [1-2] and as much as 200 Amps in the future [3]. Even though voltage is dropping, the overall power required (Volts x Amps) is increasing from today's 30 to 50 Watts to 200 Watts within the next several years. To reduce power dissipation, it is common to start and stop operation during periods of inactivity [4]. The advantage of the Multiphase Buck topology is that it is relatively simple and provides excellent transient response, high efficiency, small size, and low cost. The effective switching frequency is multiplied by the number of phases while the load is divided by the number of phases [5]. The Multiphase Buck Converter is commonly powered from a 5V or 12V bus derived from an AC-DC power supply. The trend is towards using 12V to lower the bus current and therefore reduce resistive losses in the Printed Circuit Board (PCB) and connectors.

In this paper, detail analysis and design procedures of the new proposed converter are presented in a good manner, which is nobody has tried earlier. The paper is organized as follows, Section II analyses the principle of operation. Section III describe the design process. At last, experimental results and conclusions are described in Section IV and V.

II. PRINCIPLE OF OPERATION

Ten modes are there in one complete switching cycle. On resistances of diodes and switches are considered as negligible for ease in analysis. The following is the description of each

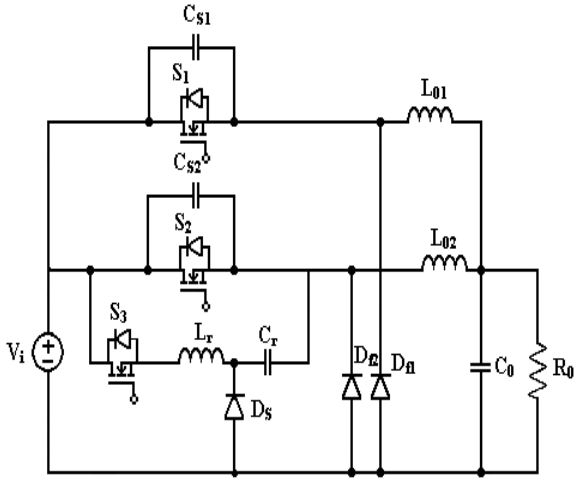

Fig. 1 The proposed converter

stage in detail. The operation waveform and mode diagrams are shown in the figs. 2 and 3 respectively

Mode 1 (t_0-t_1): At $t = t_0$, auxiliary switch S_3 start to conduct. Prior to $t = t_0$, both the freewheeling diode D_{f1} and D_{f2} carries the load current I_0. This mode end when $i_{Lr} = 0$. In this mode capacitor C_r charged to its maximum value.

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Mode 2 (t_1-t_2): At $t = t_1$, capacitor C_r start discharging through body diode of S3 and diode D_{f2}. This mode ends when capacitor voltage C_r become less than supply voltage which make provide reverse biased condition across diode D_{f2}.
Mode 3 (t_2-t_3): In this mode capacitor C_r discharge through capacitor C_{s1}. In the transient mode capacitor C_{s1} gives zero voltage across it. At the moment when voltage across C_{s1} is zero, the main switch S2 is turned on under ZVS.
Mode 4 (t_3-t_4): Now load current is shared by main switch S_2 and diode D_{f1}. This mode ends when i_{Lr} reaches to zero i.e inductor L_r transferred its energy to capacitor C_r and it is charged in the opposite direction.
Mode 5 (t_4-t_5): Current continuously increases through switch S_2 at the same order as the current through D_{f1} decreases. At the end of this mode switch S_2 is turned off under ZVS due to inductor L_{02}.
Mode 6 (t_5-t_6): With the turning off of S_2, capacitor C_r discharges its energy to load. At $t = t_6$, $V_{Cr} = 0$. The extra energy of inductor L_{02} is discharged through D_{f2}.
Mode 7 (t_6-t_7): Now again the diode D_{f2} is turned on to make the load current constant. Current through diode D_{f2} increased with sane order as current through D_{f1} decreased. At $t = t_7$, $I_{Df2} = 0$.
Mode 8 (t_7-t_8): Capacitor C_{S1} start to charge and load current remain constant. Mode ends when C_{S1} is charged to its maximum value.
Mode 9 (t_8-t_9): At $t = t_8$, main switch S_1 is turned on under ZVS due to C_{S1}. This mode end when inductor L_{01} is charged to its peak value.
Mode 10 (t_9-t_{10}): At $t = t_9$, Switch S_1 is turned off and diode D_{f1} start to conduct. At $t = t_{10}$, the auxiliary switch is turned on and new cycle start.

III. DESIGN CONSIDERATION

In order to generate a solution optimized for a particular application, the designer must consider a number of criteria. The final design approach can be determined after considering all of them and the resulting tradeoffs;

A. Number of Phases

The first thing to be considered is the optimum number of phases. Although increasing the number of phases reduces the ripple current in the input and output filters and potentially improves transient response, it also increases complexity, PCB layout difficulty, and at some point, cost. Usually, the choice is based on how many Power MOSFETs are required to efficiently handle the per phase output current. However, once it has been determined that four or more MOSFETs are required to handle the current in each phase, one should consider increasing the number of phases. This requires an additional output inductor but the increased cost and PCB area of these components tends to be offset by reductions in the cost and size of the input filter and output capacitors.

B. Current Per Phase

The performance of the MOSFETs tends to determine the optimal current per phase, which today ranges from 10 to 25A. Designs operating at lower switching frequencies, using state-of-the-art MOSFETs, and having low thermal impedance (heatsinks) tend to be in the upper end of this range. Designs targeting compact size, maximum efficiency, fast transient response, higher switching frequencies, or use of mature lower cost MOSFETs tend to be in the lower end of the range. As future generations of MOSFETs become available, it will be possible to increase the current per phase without compromising efficiency or thermal performance.

C. Transient Response

The value of the output inductor and the number of phases place a theoretical limit on the ability of the multiphase converter to slew its output current. This is due to the fact that the rate of the change of current in an inductor is equal to the voltage placed across it divided by the value of its inductance. The minimum response time to a load decrease can be calculated as follows;

$$T_{\min} = L \times \frac{(I_{\max} - I_{\min})}{V_{out}}$$

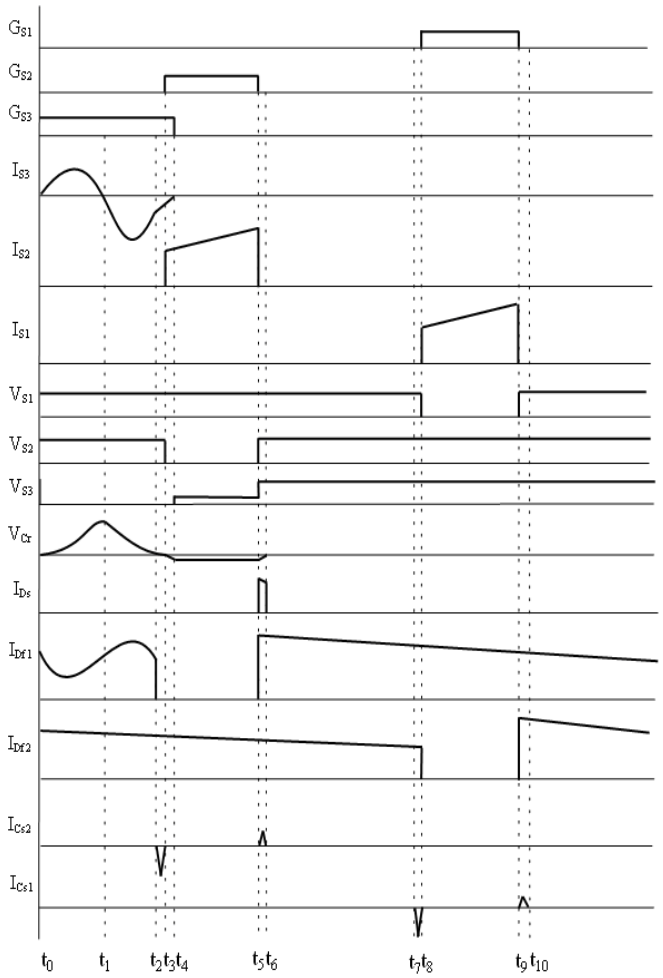

Fig. 2 Key waveforms of the proposed converter

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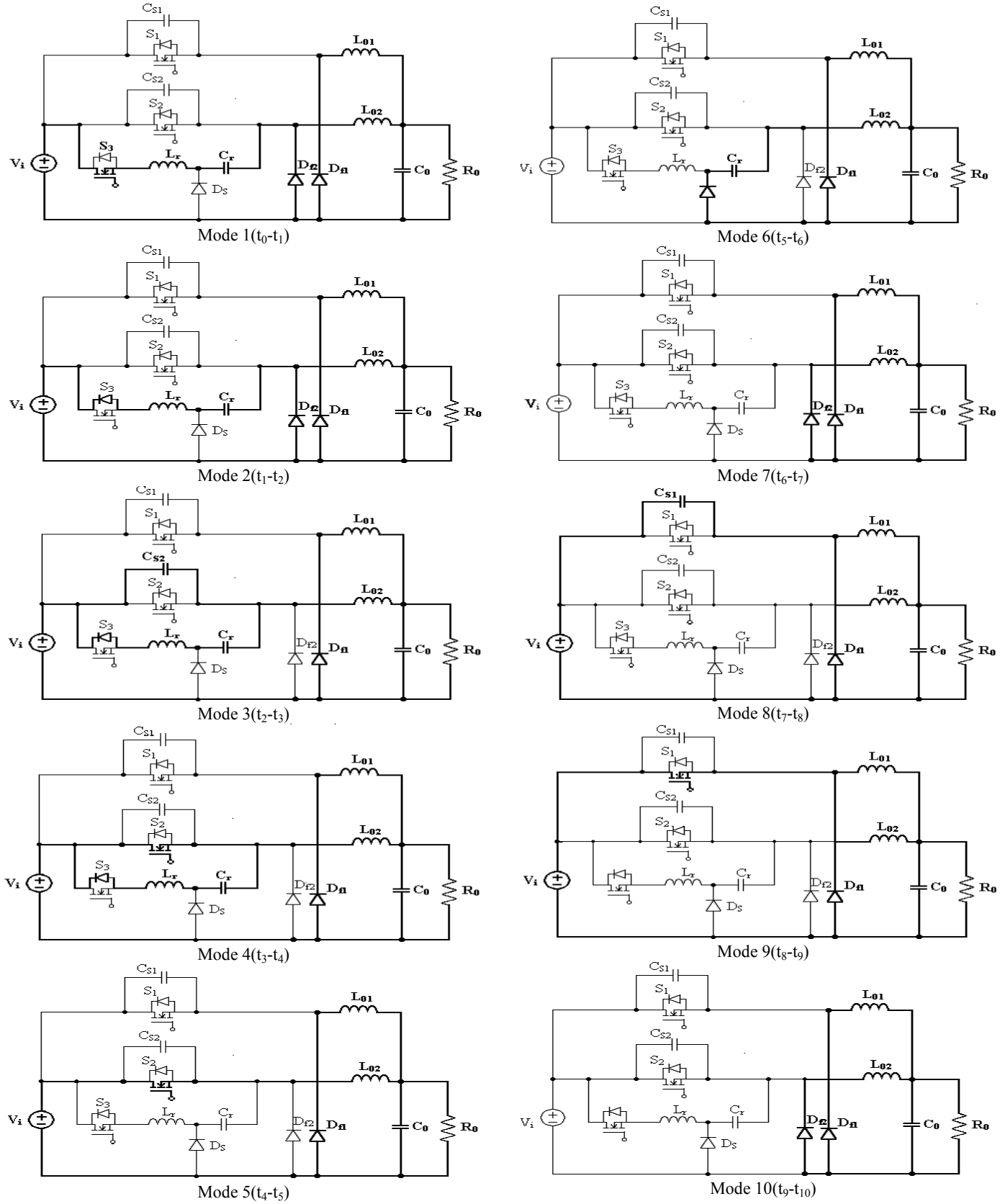

Fig. 3 Modes of operation

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Likewise, the minimum response time to a load increase can be calculated by;

$$T_{\min} = L \times \frac{(I_{\max} - I_{\min})}{V_{in} - V_{out}}$$

The theoretical minimum response time is determined by the slew rate of each inductor divided by the number of phases. This time is further increased by the response time of the PWM controller and MOSFETs.

The change in output voltage due to a load step can be calculated as follows;

$$\Delta V_o = \Delta I_o \times \frac{ESL}{\Delta I_t} + ESR + \frac{T_R}{C_o}$$

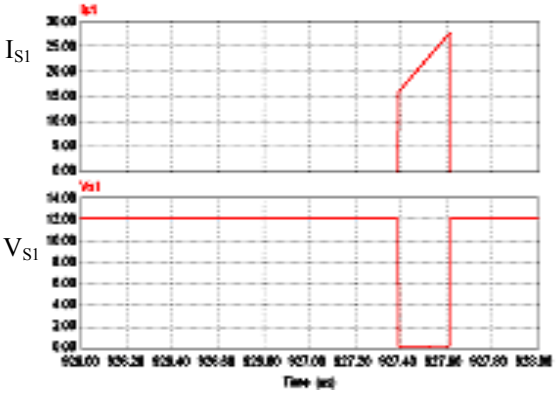
Where: delta-Io is the change in load current, ESL is the Equivalent Series Inductance, delta-It is the load current slew rate, ESR is the Equivalent Series Resistance, TR is the regulator response time and is equal to equations (1) and (2) plus the PWM response time, and Co is the total value of the output capacitor(s).

IV. EXPERIMENTAL AND SIMULATION RESULT

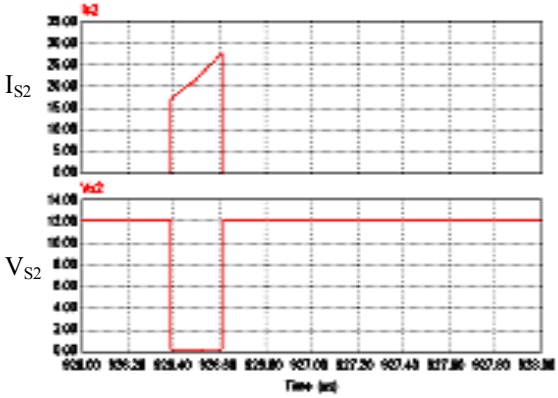
In order to test experimentally the proposed strategy, measurements have been carried out. The result is compared with that of simulated data. The proposed converter parameter are $C_{S1} = C_{S2} = 0.01$ nF, $C_r = 40$ nF, $L_r = 0.1$ µH, $L_{01} = L_{02} = 0.2$ µH, Co = 40 µF, Ro =0.1 Ω, switching frequency $f_S = 500$ kHz.. Simulated and experimental results are shown in the fig. 4 and fig. 5.

A. *Simulation Results*

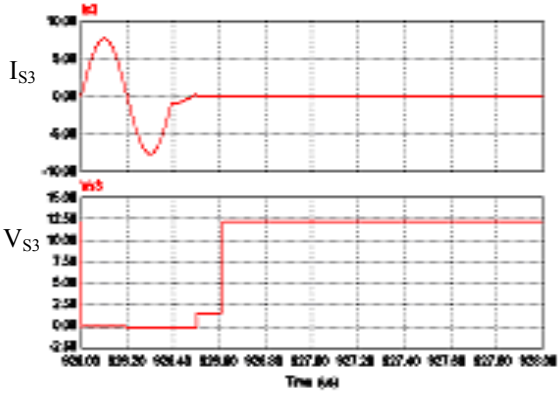
The proposed topology is simulated with PSIM 6.0 software. All switches are operated with the help of proper control techniques. The simulated converter delivers a load of 100W with efficiency of 97.26 %. In fig. 6 graph between efficiency and no. of phases is shown by taking the experimental data.. With change in no. of phases how the efficiency varies is shown in the fig. 6. Here in this topology two phases with soft switching technique is taken into consideration. Reduction of switching loss and improvement of efficiency by the use of ZVS can be clearly seen from the figure 7, where efficiency with ZVS and without ZVS is shown. In without ZVS case, auxiliary switch is not used.



(a)



(b)

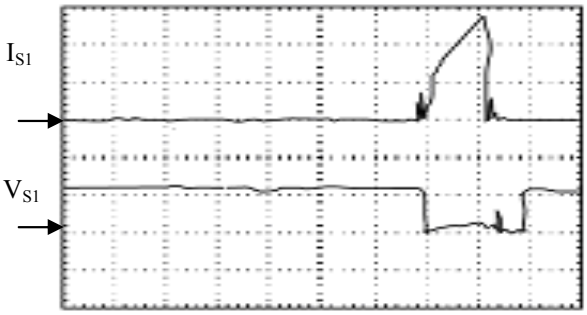


(c)

Fig. 4 Simulated current and voltage waveform of three MOSFET switches S_1, S_2, and S_3 respectively

B. *Experimental Results*

There is deviation in experimental waveforms from simulated waveforms. One prototype of multiphase converter is taken for experimental purpose. Soft switching losses are reduced by using soft switching techniques, but some conduction losses in switches as well as in other elements are still present there which make the experimental waveforms different from simulated waveforms .



(a)

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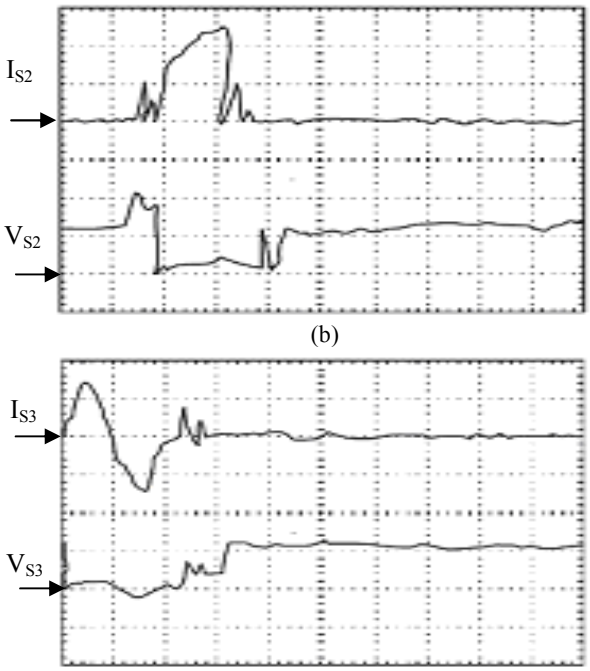

Fig. 5(a). Experimental voltage and current waveforms of switch S_1 (V_{S1}: 10 V / div, I_{S1} : 10 A / div), 5(b) Experimental voltage and current waveforms of switch S_2 (V_{S2}: 10 V / div, I_{S2} : 10 A / div), 5(c) Experimental voltage and current waveforms of switch S_3 (V_{S3}: 10 V / div, I_{S3} : 5 A / div),

V. CONCLUSION

The proposed converter designed has several features and advantages: high efficiency, high power density, least size due to multiple phases, cheaper and faster switching frequency of 500 kHz. With increased in number of phase efficiency can be improved.

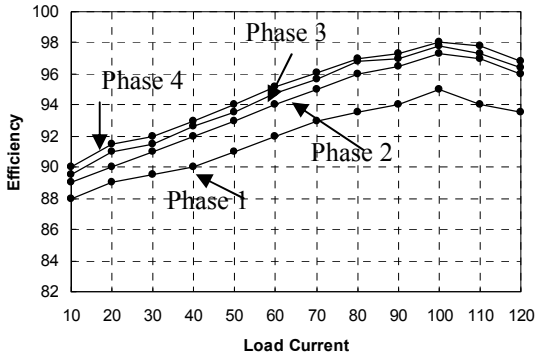

Fig. 6 Efficiency Vs Load current with respect to no. of phases.

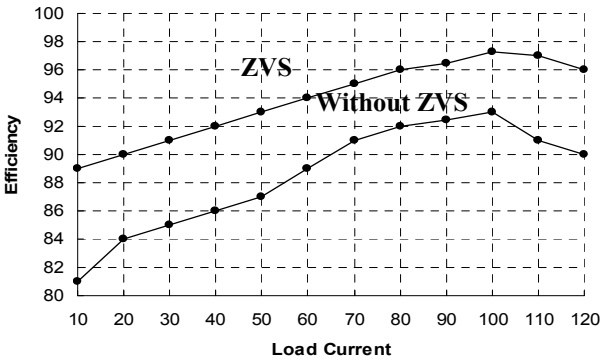

Fig. 7 Graph between efficiency and load current

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