A Novel Technique to Reduce the Switching Losses in a Synchronous Buck Converter

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***Abstract*--This paper proposes a zero-voltage transition (ZVT) PWM synchronous buck converter, which is designed to operate at low output voltage and high efficiency typically required for portable systems. To make the DC-DC converter efficient at lower voltage, synchronous converter is an obvious choice because of lower conduction loss in the diode. The high-side MOSFET is dominated by the switching losses and it is eliminated by the soft switching technique. Additionally, the resonant auxiliary circuit designed is also devoid of the switching losses. The suggested procedure ensures an efficient converter. Using an example design, the converter operation is explained and analyzed.**

Index Terms-- **DC-DC Converter, Switching loss, Synchronous Buck, ZVT**

I. Introduction

THE next generation of portable products, such as personal communicators and digital assistants, will have to provide long hours of operation between battery charges. A key element in this task, especially at low output voltages that future microprocessor and memory chips will need, is the synchronous rectifier. A synchronous rectifier is an electronic switch that improves power-conversion efficiency by placing a low-resistance conduction path across the diode rectifier in a switch-mode regulator. MOSFETs usually serve this purpose [1], [2].

However, higher input voltages and lower output voltages have brought about very low duty cycles, increasing switching losses and decreasing conversion efficiency. So in this paper, we have optimized the efficiency of the synchronous buck converter by eliminating switching losses using soft switching technique [3].

The voltage-mode soft-switching method that has attracted most interest in recent years is the zero voltage transition. This is because of its low additional conduction losses and because its operation is closest to the PWM converters. The auxiliary circuit of the ZVT converters is activated just before the main switch is turned on and ceases after it is accomplished.

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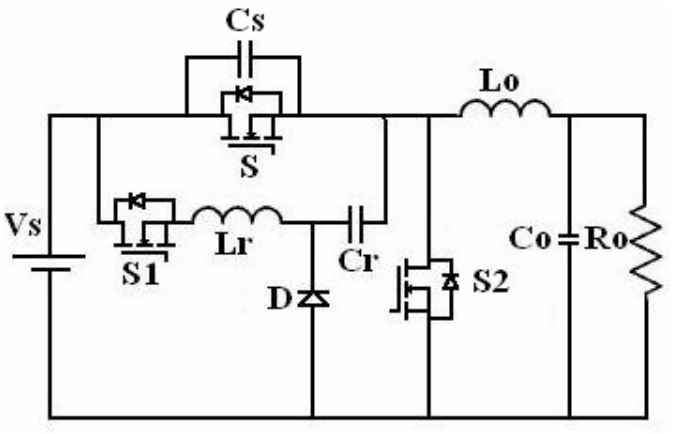


Fig. 1. The proposed converter.

The additional conduction losses are therefore substantially reduced. Moreover, it has little effect on the converter operation characteristics. Many techniques to reduce switching losses in high power have been proposed using both active and passive snubbers. Reducing switching losses for low power circuit such as synchronous buck is not known to be present in the literatures [4] – [7]. The converter shown in Fig.1 is designed for a low voltage, high current circuit and found to be highly efficient.

Hence, this paper presents a new class of ZVT synchronous buck converter. By using a resonant auxiliary network in parallel with the main switch, the proposed converters achieve zero-voltage switching for the main switch and zero-current switching for the auxiliary switch without increasing their voltage and current stresses.

The paper is organized as follows. The next section gives a short description of the proposed circuit followed by review of the various modes of operation with their key waveforms and the representation of their equivalent operation modes. Section III presents the design considerations and section IV includes simulation results to illustrate the features of the proposed converter scheme. Section V includes some conclusions.

II. Modes Of Operation

The circuit scheme of the proposed new ZVT synchronous buck converter is shown in Fig.1. The auxiliary circuit consists of switch S_2, resonant capacitor Cr, Resonant inductor Lr. The auxiliary circuit operates only during a short switching-transition time to create ZVS condition for the main switch. The body diode of the main switch is also utilized in the converter.

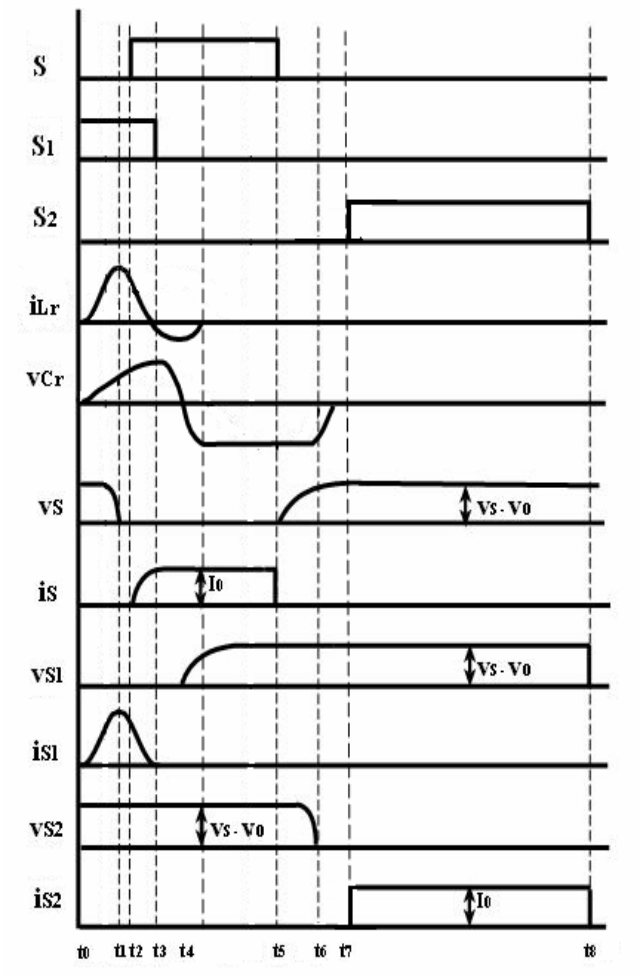


Fig. 2. Converter waveforms.

A high frequency schottky diode D is used for discharging the capacitor voltage to the output, which happens before the turn on of the synchronous switch. The various modes of steady-state converter operation that goes through during a switching cycle are explained in this section of our paper. Typical waveforms of the converter are shown in Fig. 2, and the equivalent circuit for each mode of operation is shown in Fig. 3. For the sake of simplicity, output inductor, Lo, can be considered to be large enough to be a constant current source, Io. The description of each mode is presented as follows:

Mode 1 (t_0, t_1): At t_0, the switch S_1 is turned on. S_1 realizes zero-current turn-on as it is in series with the resonant inductor Lr. The current through Lr and Cr increases. At the same instant, the capacitor Cs which was already charged to the supply voltage will start discharging through Lr, Cr, Cs and S_1. The resonant network consists of Lr_1, Cr and S_2. The mode ends at $t = t_1$, when the capacitor across the main switch Cs is completely discharged.

Mode 2 (t_1, t_2): V_S is fully discharged and the body diode of the main switch begins to conduct at t_1 as i_{Lr} is greater than the output current. This mode ends when the body diode of the main switch is off. This happens when resonant current falls to the load current (iLr=Io).

Mode 3 (t_2, t_3): At t_2, the main switch S is turned on by ZVS. During this stage the growth rate of i_s is determined by the resonance between Lr and Cr. The resonant process continues in this mode and the current through i_{Lr} starts to decrease. This mode ends when S_1 is turned off and iLr falls to zero.

Mode 4 (t_3, t_4): At t_3, the body diode of S_1 starts to conduct. The resonant current iLr flows in the reverse direction, reaches a maximum value and falls to zero. This mode ends when body diode of S_1 is turned off.

Mode 5 (t_4, t_5): Since the body diode has turned off, only the main switch carries the load current. There is no resonance in this mode and the circuit operation is identical to a conventional PWM buck converter.

Mode 6 (t_5, t_6): At $t = t_5$, the main switch S is turned off with ZVS. The capacitor Cs starts charging through source Vs and load.

Mode 7 (t_6, t_7): The schottky diode D starts conducting. The resonant energy stored in the capacitor Cr starts discharging to the load through the high frequency schottky diode D for a very short period of time, hence body – diode conduction losses and drop in output voltage is too low. This mode finishes when Cr is fully discharged and Cs is fully charged.

Mode 8 (t_7, t_8): At $t = t_7$, switch S_2 is turned on as soon as Cr is fully discharged. Dead time loss is negligibly small compared to the conventional synchronous buck converter. During this mode, the converter operates like a conventional PWM buck converter until the switch S_2 is turned on in the next switching cycle.

III. Design Considerations

A. Inductor selection

The lower inductor values are best for high frequency converters, since the peak-to-peak current increases linearly with switching frequency. A good rule of thumb is to select an inductor that produces a ripple current of 10 to 30% of full load DC current. Too large an inductance leads to poor loop response, and too small an inductance leads to high AC losses.

B. Resonant capacitor selection

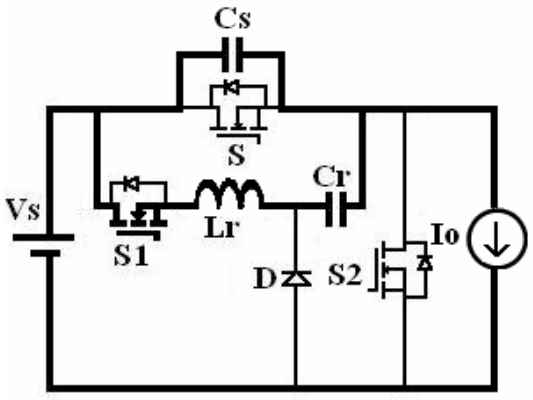
Since the current in the switching MOSFET is pulsating, a large resonant capacitor is used.

C. Output capacitor selection

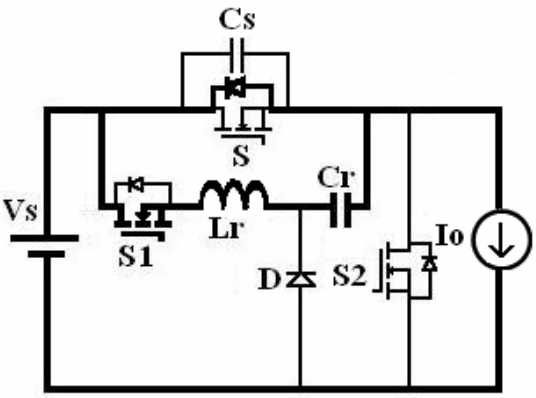
The output capacitor is chosen to minimize output noise voltage and to guarantee regulation during transient loads. For a low value of inductance, bulk storage may not be necessary, in which case design using only ceramic capacitors may be achieved.

D. Feedback loop design

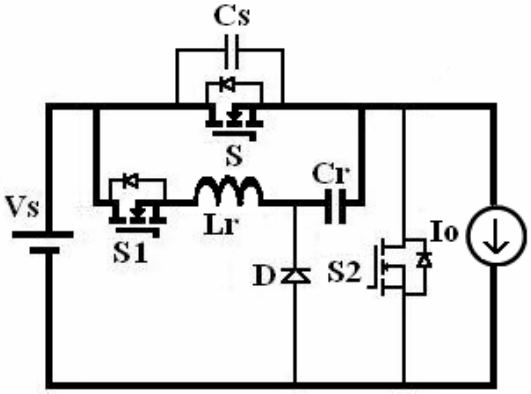
The converter power stage frequency response frequency response characteristics are determined, and then based on the resulting curves; a compensation network is designed to give the desired result. The L-C filter gives the output voltage a double pole response to the output of a compensation network. The compensation network can be designed to have a crossover frequency either above or below the L-C filter's double pole frequency.



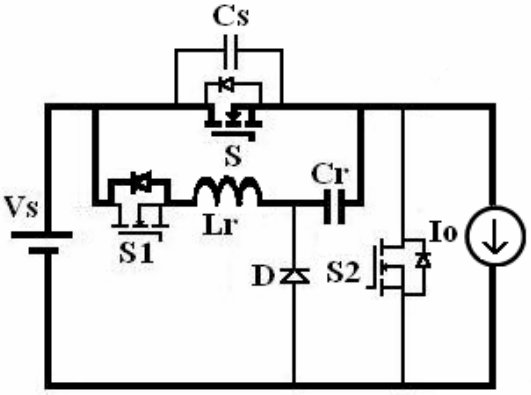
Mode 1 (t0-t1)



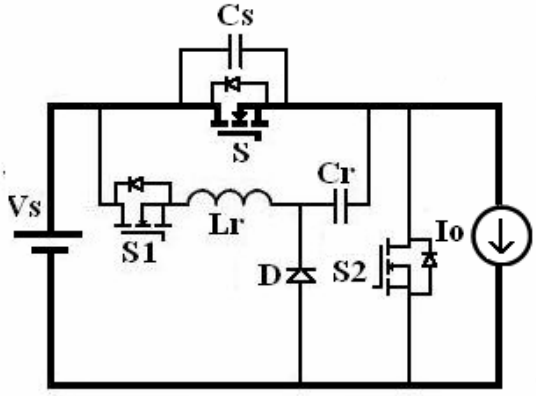
Mode 2 (t1-t2)



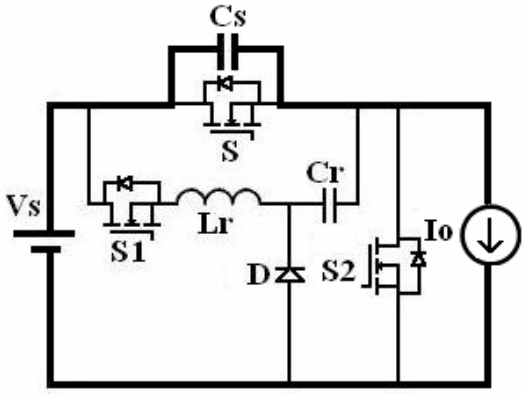
Mode 3 (t2-t3)



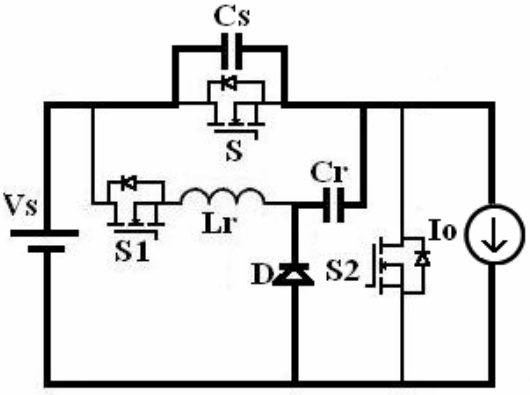
Mode 4 (t3-t4)



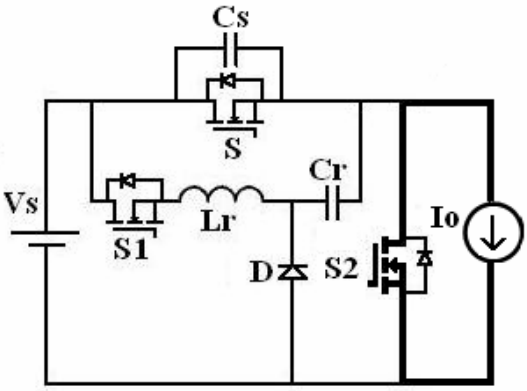
Mode 5 (t4-t5)



Mode 6 (t5-t6)

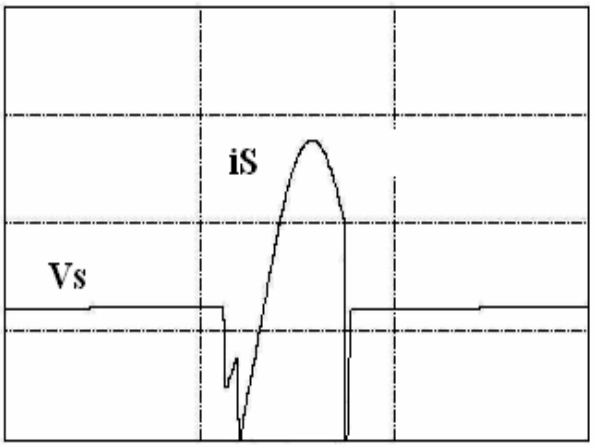


Mode 7 (t6-t7)

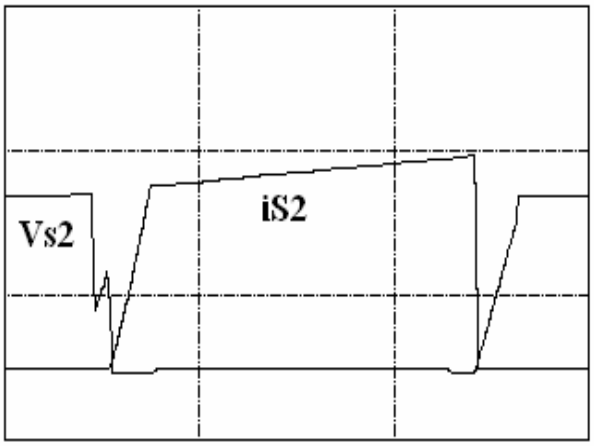


Mode 8 (t7-t8)

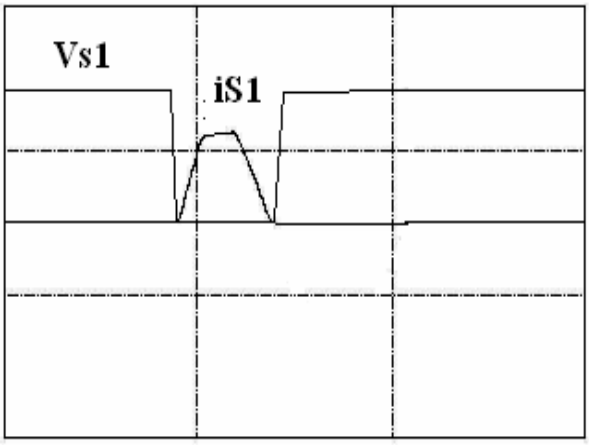
Fig. 3. Converter operation modes.



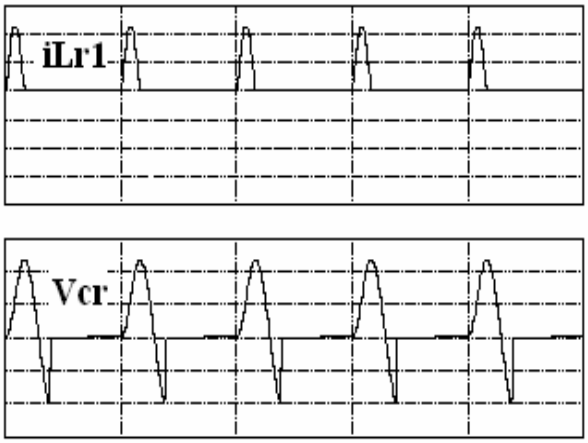
Main switch S : vS , iS – (5V, 5A)/div



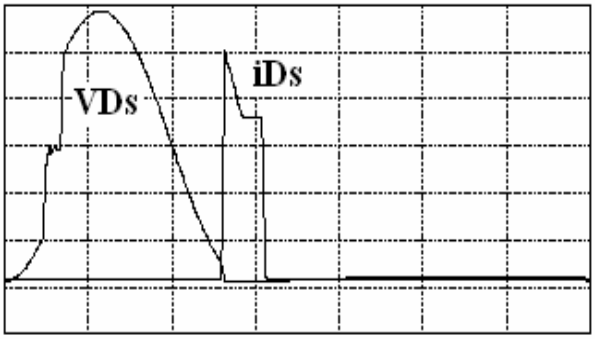
Synchronous switch S2: vS2, iS2 – (2V, 2A)/div



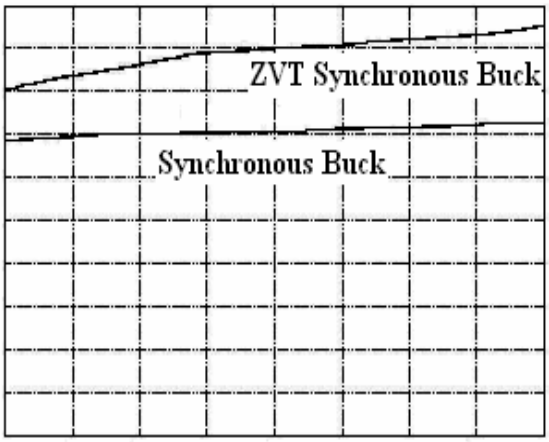
Auxiliary switch S1 : vS1 , iS1 – (5V, 5A)/div



iLr1, vCr - (3V, 3A)/div



Schottky diode Ds: vDs, iDs – (6V, 6A)/div



X-axis : Output power - 5W/div
Y-axis : Efficiency - 80 - 100%

Fig. 4. Simulation waveforms

E. MOSFET Selection

A method to choose the MOSFETs for the converter is to compare the power dissipation values for a number of different MOSFET types. Usually, a low on-state drain resistance MOSFET is chosen for the synchronous Rectifier, and a MOSFET with a low gate charge is chosen for the switches.

IV. Results

The newly proposed converter operates with an input voltage Vs = 12V, output voltage Vo = 3.3V, load current of 12A and a switching frequency of 1MHz and the circuit parameters are: output inductance Lo = 1µH, output capacitance Co = 30µF, resonant inductors Lr = 60nH, 90nH, resonant capacitor Cr = 0.1µH, capacitor Cs =0.5nF.

The switching loss of a synchronous buck converter without the soft-switching technique for the above parameters accounted for 50 % of the total losses. High side switching losses alone accounted for 45% of the total losses. So eliminating switching losses on high side becomes prime importance.

Fig. 4 shows the simulation waveforms of this converter. All the waveforms except the efficiency curve represents a time period of one switching cycle, which is 1µs in this case. The amplitudes are denoted below each of their waveforms respectively.

A. Main Switch S

It is noted from the figure that the main switch operates with the soft switching technique. The converter has not exceeded the voltage and current limits in the main switch. The conduction time of the switch can also be noticed, which is very low appropriate to the design parameters.

B. Auxiliary Switch S_1

It is noted from the figure that auxiliary switch also operates with the soft switching. The shape of the figure is identified to confine much with the theoretical waveform. The auxiliary switch is active only for a short period of time, which is verified by its conduction period and it's too small. Also, this switch's current and voltage are well within the operating limits.

C. Schottky Diode D

The schottky diode works for a very short period to discharge the resonant capacitor Cr. A high-frequency schottky diode which is available at high-current, low voltages can be used. The conduction of schottky diodes may cause a considerable drop in output voltage for low power circuits but due to the advancement in semiconductor techniques, schottky diodes are also now available with a low forward voltage drop for high frequency circuits.

D. Synchronous switch S_2

The synchronous switch also has characteristics similar to the switches S, S_1. They operate within the safe limits and it can be noted here, the conduction period of S_3 is more confining to the design values and it operates at a low power when compared to the other switches.

E. Efficiency curve

The ZVT synchronous buck converter is found to be more efficient when compared to the conventional synchronous buck converter. The efficiency value is found for different values of output power. The high efficiency concludes the correctness of the design values.

V. Conclusion

The concepts of ZVT used in high power were implemented in synchronous buck converter and it was shown that the switching losses in synchronous buck were eliminated. Hence the newly proposed ZVT synchronous buck is highly efficient than the conventional converter. The additional voltage and current stresses on the main devices do not take place, and the auxiliary devices are subjected to allowable voltage and current values. Moreover, the converter has a simple structure, low cost and ease of control.

VI. References

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