Novel Four-Stage Comparator With High Speed and Low Kickback Noise

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***Abstract*—The implementation of CMOS four-stage comparator with improved speed, kickback noise and resolution is the subject of this paper. After performing functional verification, it is observed that cascading of pre-amplifiers can achieve a faster speed, the proposed comparator offers higher speed of operation, as compared to typical dynamic comparators referred in this paper. Furthermore, the noise cancelling mechanism of a complementary input pair is used at the preamplifier stage in the proposed four-stage comparator, which is identicalto that of the referred three-stage comparator. The kickback noise is considerably reduced compared to that in the three stage comparator by introducing a new method for kickback noise cancellation which will stabilize the operating point. The proposed comparator also offers a better resolution compared to the state-of-the-art work, during the regeneration stage, it significantly helps to boost the speed even more. Simulated results show that the proposed four-stage comparator reduces the delay and kickback noise by 45.53 % and 32.35 % respectively as compared to Zhuang's Comparator. All simulations are run on the same technology node TSMC 180nm for fair comparison with the existing designs. These advantages are obtained at the cost of increased energy per comparison and input referred noise marginally.**

***Index Terms*—Comparator, slew rate, regeneration, low kickback.**

I. Introduction

From many decades almost all communications are happening in the digital mode, it may be the internet of things (IOT) for specific applications or the mobile communications for generic applications, for that to happen the information needs to be converted to digital form from analog signal as digital signal has less interference from noise. For the fast conversion of information from analog form to bit stream (digital) form we require SAR ADC, and the comparator is main building block of it [1] - [3]. So, there is always a need to make the conversion faster and less noisy for accurate and redundant communication.

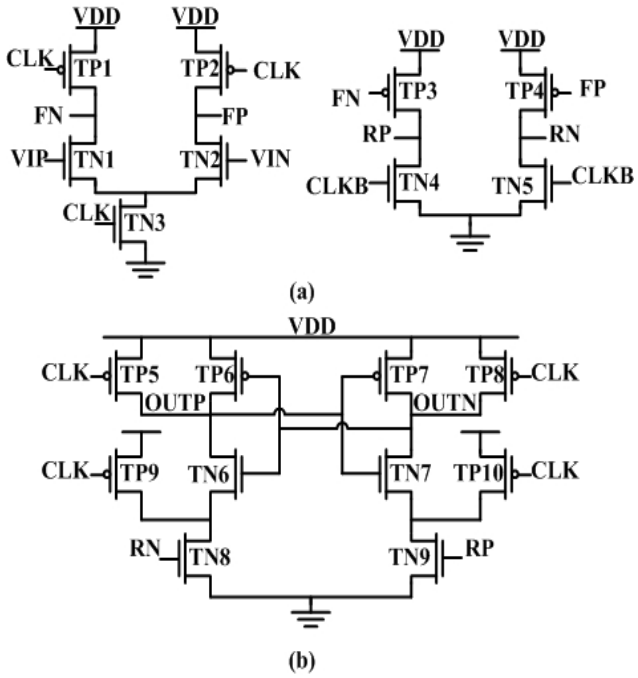

Fig. 1. Brandolini's three-stage comparator in [8]. (a) Preamplifier stages. (b) Latch stage.

There are many circuits proposed in past years. Earlier there used to be two stage comparators reported in [2] - [7] which were able to deliver higher speed and low kickback compared to single stage comparators introduced before them. These two stage comparators also delivered rail-to-rail outputs and almost zero static power. It also has certain disadvantages as two stage comparators also delivered rail-to-rail outputs. It also has certain disadvantages as it lesser input resolution which cannot detect the smaller differential voltages and it also has larger input referred noise in some of them.

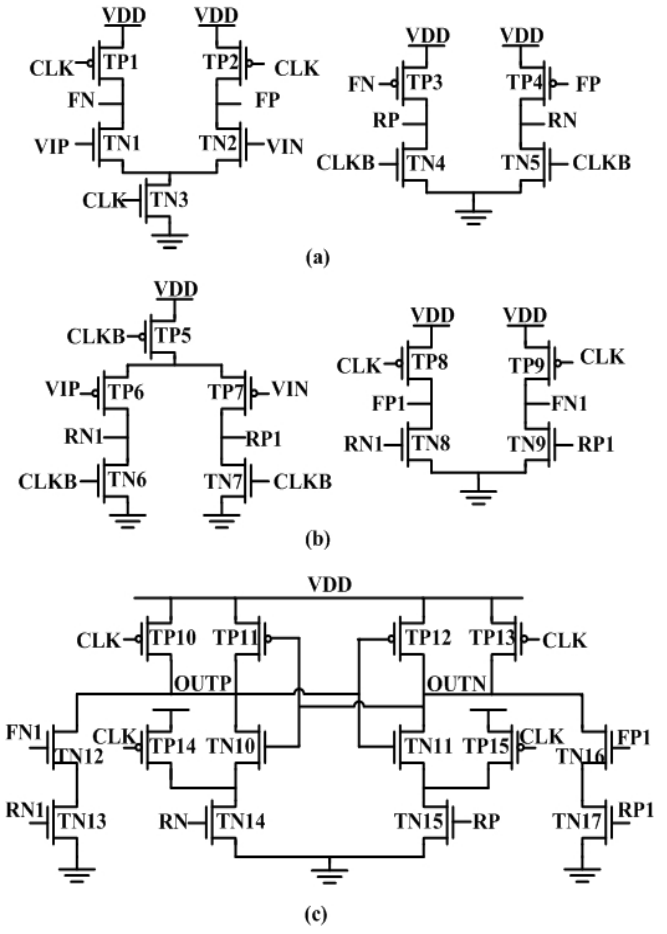

Fig. 2. Zhuang's three-stage comparator in [10]. (a) Preamplifiers with NMOS input pair. (b) Preamplifiers with PMOS input pair. (c) Latch stage.

Later in Brandolini's [8] three-stage comparator with single NMOS input pair and addition of one more preamplifier derived from dynamic inverter and cascaded in NORA logic fashion, meaning alternate NMOS-PMOS dynamic input networks to avoid problems associated with dynamic cascading shown in Fig. 1. The Brandolini's comparator with the additional preamplifier at 2nd stage has given a higher magnitude of slew rate or amplification at the second stage which has improved the frequency of operation further. But it has not introduced any new method for reduction of kickback noise, addition of a preamplifier from the method mentioned by Figueiredo in [9] has reduced kickback noise by a very minute amount. Also there is no improvement is resolution.

The Zhuang's comparator shown in Fig. 2, has proposed a new method for kickback noise cancellation, by introducing PMOS input pair (TP6, TP7) along with NMOS input pair mentioned in Brandolini's work. Along with the regenerative latch, Zhuang's comparator also has two discharging current paths given by TN12, TN13, TN16 and TN17 to make the regenerative action fast.

This paper is organized as follows. Section II discusses method adopted for reduction of kickback noise. Section III discusses the operation of Zhuang's comparator. Section IV discusses the proposed comparator structures and operation. Section V includes the comprehensive report of simulated results. Section VI includes the conclusion of this literature.

II. Reduction of Kickback Noise

A. Method Adopted for Kickback Noise Reduction in Zhuang's Comparator

As shown in Fig. 3, there is no current flow in next stage of preamplification from the NMOS and PMOS input pairs both. So there is current flow only for charging and discharging of the drains of the input pair transistors, there is kickback noise in the NMOS input pair because of current flow from drain of TN3 and TN4 transistors towards the gate through Cgd and in the case of PMOS input pair from gate to drain of TP1 and TP2 through Cgd. The kickback noise at both the input pairs are cancelled to a large extent. But due to transistorized and capacitive mismatch there is still some kickback noise present.But this was the best method for cancellation in state-of-the-artwork.

B. Method Proposed for Kickback Noise Reduction in Proposed Design

In the proposed methodology, attempt is made to bring the kickback noise as low as possible. Zhuang's method is adopted along with psuedo Clk inputs at TN1 and TN2 named CLKbias in Fig. 4 (a). CLKBias reduces the large change in voltages at FN and FP thus reduces the kickback noise at gates of TP1 and TP2 and therefore it becomes equivalent to that obtained at gates of TN3 and TN4 cancelling most of the kickback noise. It also increases the resolution of the circuit to a great extent. While Fig. 4 (b) is same as existing. Fig.5-6 shows the Clock inputs for Zhuang's comparator and the proposed comparator. The Optimum CLKbias swing can be observed from the behaviour of circuit for different CLKbias swings shown in Fig. 7-8 for the proposed comparator.

III. Zhuang's Three Stage comparator

A. Review of Brandolini's Three Stage Comparator

Fig. 1 shows the Brandolini's three stage comparator with NMOS input pairs. The two stages are preamplifiers to increase the slew rate of inputs to the regenerative latch. It can be seen as the common mode input at the first stage keeps TN1 and TN2 in the linear mode so flow of current is less through them and FN and FP outputs will discharge slowly to ground, but when they are applied to the next stage dynamic inverter formed by TN4, TN5, TP3 and TP4 this discharged outputs FN and FP pulls the outputs RN and RP to VDD very fast and thus these outputs are applied to the third stage of the regenerative latch and thus the comparison action is fastened.

B. Structure and Operation of Zhuang's Three Stage Comparator

In the Zhuang's comparator shown in Fig. 2 it has another PMOS input pair formed by TN6-TN9 and TP5-TP9 in addition to that shown in Brandolini's structure to cancel the kickback noise. The operation of Zhuang's comparator is as follows.

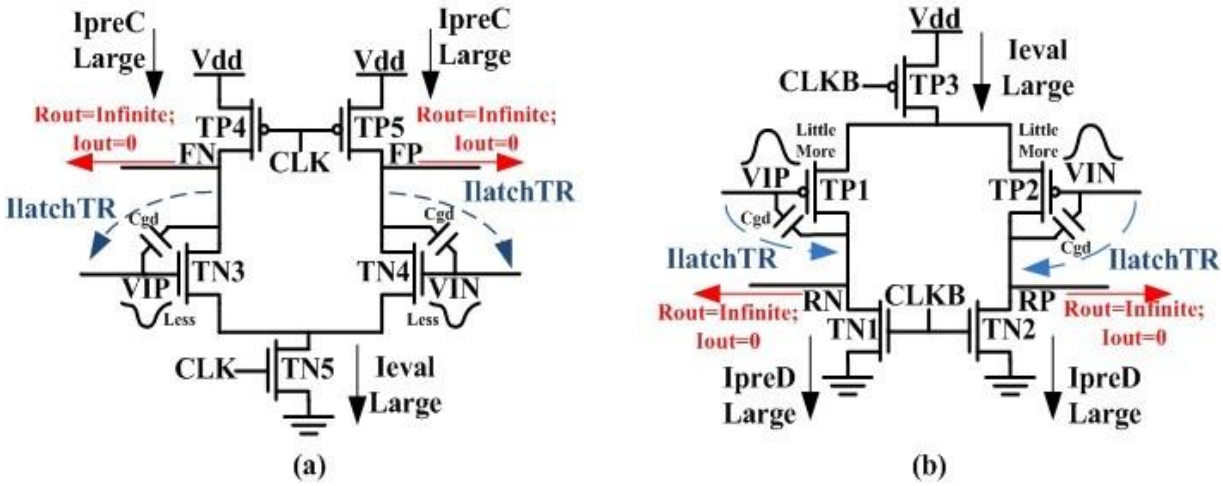

Fig. 3. Cancellation of kickback noise in Zhuang's comparator. (a) Kickback noise in NMOS input pair. (b) Kickback noise in PMOS input pair.

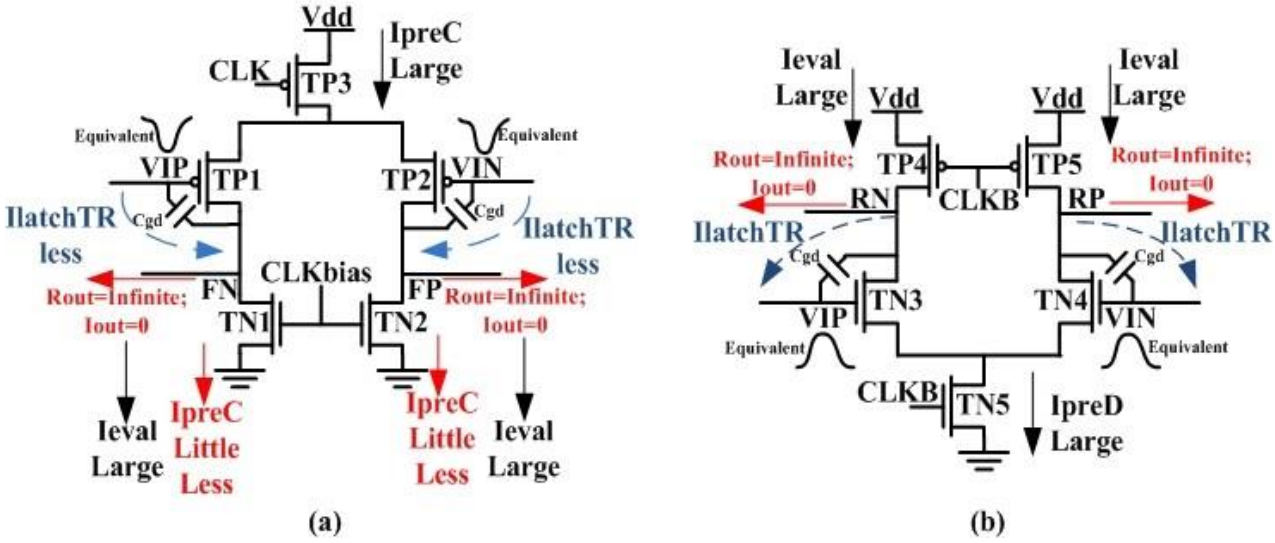

Fig. 4. Cancellation of kickback noise in proposed comparator. (a) Kickback noise in modified PMOS input pair. (b) Kickback noise in NMOS input pair.

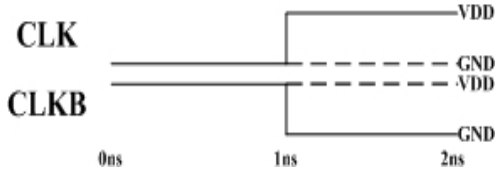

Fig. 5. Clock inputs for Zhuang's comparator.

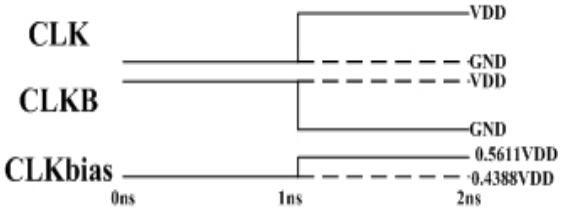

Fig. 6. Clock inputs for proposed comparator.

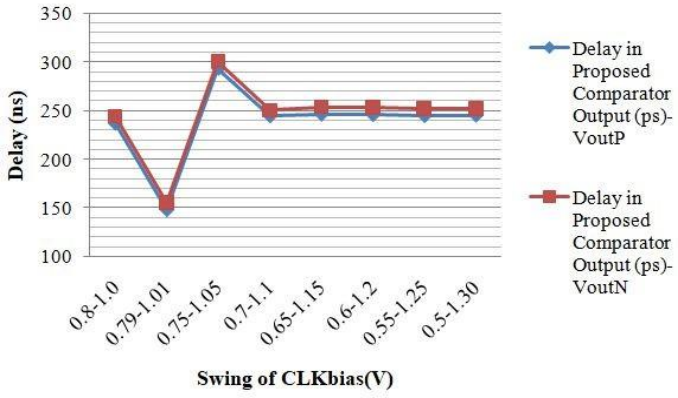

Fig. 7. Delay versus swing of CLKbias.

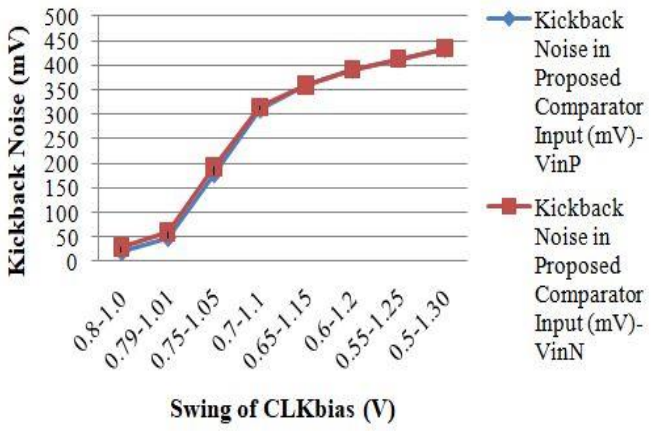

Fig. 8. Kickback noise versus swing of CLKbias.

During the reset phase, CLK=0 and CLKB=1. All falling outputs (FN,FP, FP1 and FN1) of the preamplifiers are reset to VDD, and the rising outputs (RP, RN, RN1 and RP1) are reset to ground. During this phase TN14-15 are switched off and both outputs OUTP and OUTN are reset to VDD through TP10 and TP13 respectively. During this phase TN13 and TN17 are also off thus ensures no static current flow in the extra path TN12, TN13, TN16 and TN17.

During the amplification phase, CLK switches to logic 1(VDD) and CLKB switches to 0(Ground), all falling preamplifier outputs fall to ground and the rising outputs rise to VDD. So TN14-TN15 are turned ON and depending on the value of differential voltage the rising inputs RN and RP to the regenerative latch will rise with different slew rates and discharging of the outputs will happen. Depending on this the regeneration will happen and OUTP will be High for positive differential voltage and low for a negative differential voltage, output on OUTN will be opposite that of OUTP. The extra path TN12, TN13, TN16 and TN17 are turned ON for some time and it passes a differential voltage which speeds up the regeneration.

IV. Proposed Four-Stage Comparator

Fig. 9 shows the proposed four-stage comparator. Along with the Zhuang's comparator [10] with NMOS input pairs at the regenerative latch and the extra discharging paths formed by TN18-TN21, additional static inverters are added at the outputs of the two stage preamplifiers to make the preamplification a three stage and overall makes the comparator a four stage to enhance the speed of operation [12]. Along with this a separate attenuated clock CLKbias is used at the PMOS input pair discharging circuitry. Fig. 10-11 shows the transientsimulated outputs of Zhuang's and proposed comparators.

The operation of the comparator occurs in two stages, the reset and the evaluation stage: In the reset phase, CLK=0, CLKB=1 and CLKbias=0.4388 VDD, during this phase TP3 and TN9 are ON, TP8 and TP9 are OFF but TN1 and TN2 are

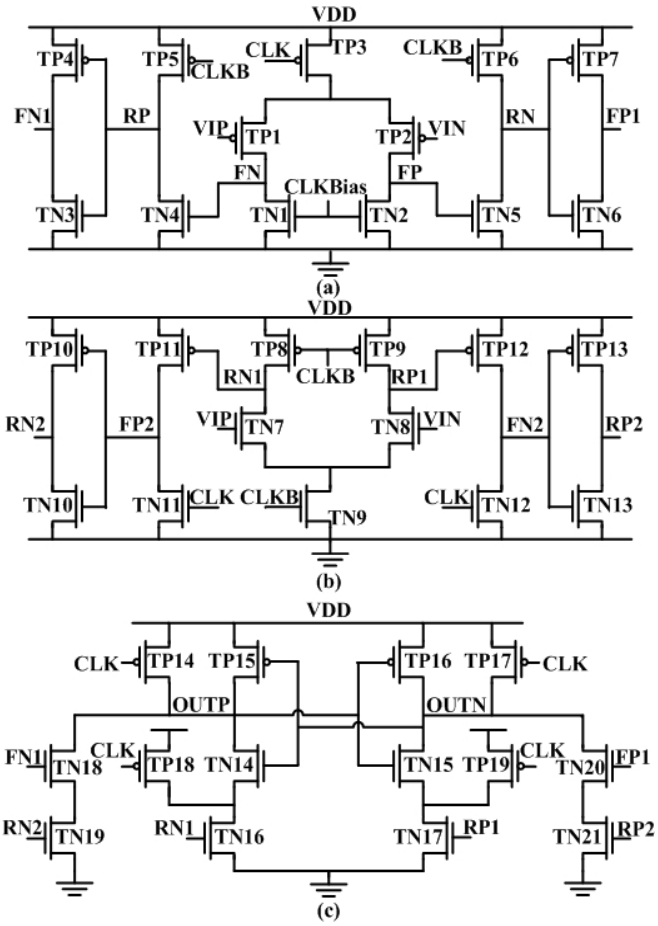

Fig. 9. Proposed four-stage comparator. (a) Preamplifiers with PMOS input pair. (b) Preamplifiers with NMOS input pair. (c) Latch stage.

partially ON because of the CLKbias input unlike that of the Zhuang's Comparator, thus FN and FP nodes are pulled up to VDD through TP1 and TP2 but parallelly they are discharging through TN1 and TN2 maintaining the static discharging path from rail to rail which will stabilize the current. And RN1 and RP1 nodes are pre-discharged to ground.

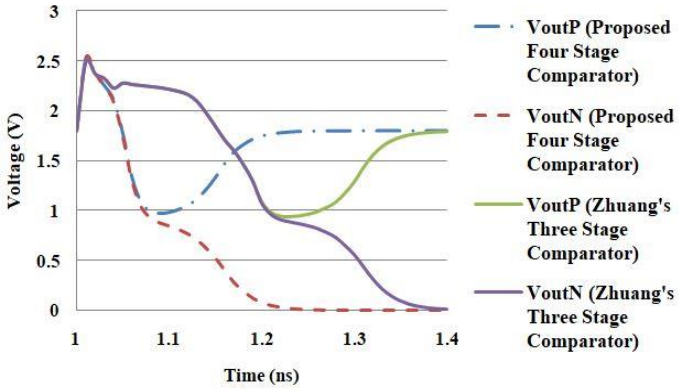

Fig. 10. Delay after transient simulation of Zhuang's and proposed comparator.

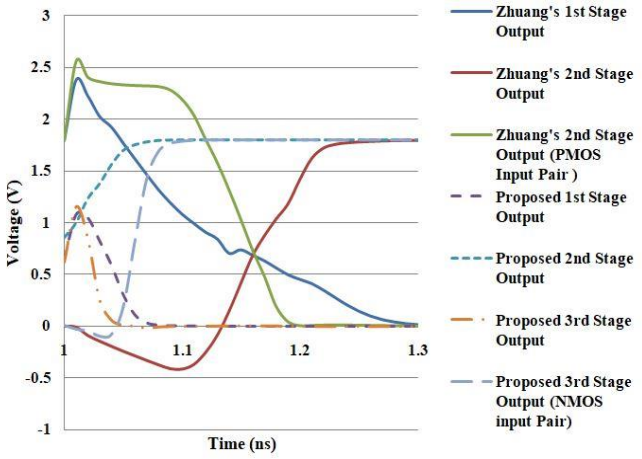

Fig. 11. Stagewise preamplifier outputs of Zhuang and proposed comparator.

During the evaluation phase, CLK=1, CLKB=0 and CLK-Bias=0.5611 VDD, TP3 and TN9 are OFF, TN1 and TN2 are partially ON discharging the outputs FP and FN slower than that if a full swing clock would be added, TP8 and TP9 transistors are ON and charging the RP1 and RN1 nodes with a higher slew rate compared to the discharging of FP and FN nodes. These outputs are fed to next stage dynamic inverter and next to next stage static inverter and then are fed to the regenerative latch to get the desired detection.

Values of the lesser swing clock is kept specifically as CLKbias=0.5611 VDD for high and CLKbias=0.4388 VDD because the large voltage variation has to be reduced at the drains of PMOS input pairs shown in Fig. 4 (a). Also it could not be brought down below CLKbias=0.5611 VDD for high and brought above for CLKbias=0.4388 VDD because it will not evaluate. This change in clock inputs from Zhuang to proposed comparator can be seen in Fig. 5-6.

V. Comparison of Simulation Results

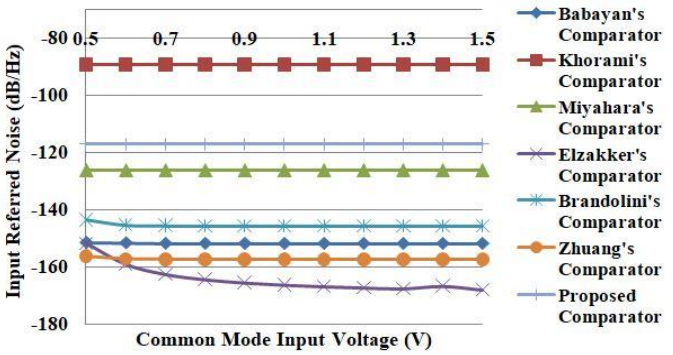

Fig. 12. Simulated input referred noise in dB/Hz with respect to the common mode input voltage.

This section compares the four-stage comparator proposed in this work with the state of the art work. For a fair comparison all the comparators are simulated on 180nm technology with a supply voltage of 1.8 V. Also the aspect ratios used in all the comparators are same.

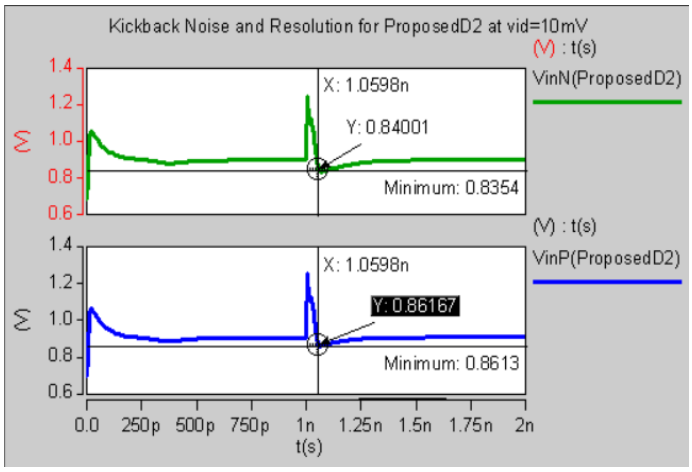

Fig. 13. Calculation of kickback noise and resolution in proposed comparator.

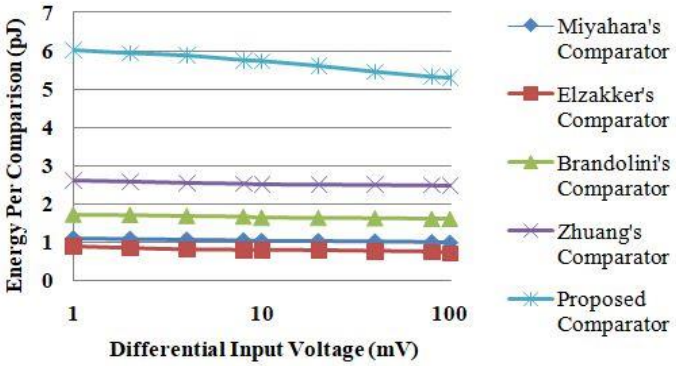

Fig. 14. Energy required per comparison versus differential input voltage.

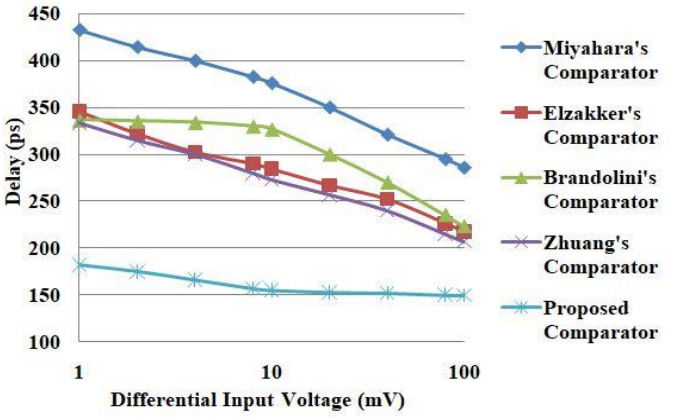

Fig. 15. Simulated delay versus differential input voltage.

The input referred noise for all the comparators are simulated at 0.5 GHz frequency. Table I discusses the performance parameters of state-of-the- art works.

Fig. 12 shows the variation of input referred noise in dB/Hz with respect to variation in common mode input voltage, all the noise inputs are evaluated at 0.5 GHz and compared, found that it is -126.27 dB/Hz, -165.5 dB/Hz, -145.6 dB/Hz, -157.32 dB/Hz, -117.134 dB/Hz for Miyahara's, Elzakker's, Brandolini's, Zhuang's, Proposed Comparator respectively at

TABLE I
COMPARISON OF RESULTS WITH STATE-OF-THE-ART WORKS

	Babayan [4]	Khorami [5]	Miyahara [6]	Elzakker [7]	Brandolini [8]	Zhuang [10]	Proposed Comparator
Technology (nm)	**180**						
Supply Voltage (V)	**1.8V**						
Kickback Noise (mV) for Vid=10mV	237.2 239.1	287.2 283.3	173.1 176	155.6 158.7	145.5 148.5	88.7 84.8	60 48.33
Difference in the two Inputs(VIP and VIN) in mV while measuring Kickback through resistors for Vid=10mV	8.1	7.7	7.1	7	7.1	6.3	21.66
Energy Per Comparison (pJ) at 500MHz for Vid=1mV	2.72	1.30	1.10	0.88	1.725	2.60	6.0
Delay for Vcm=0.9V and Vid=1mV	681.7 714.9	324.1 376.6	402.2 433.4	324.8 346.3	336.9 330.6	333.6 327.3	181.7 174.2

common mode input voltage of 0.9 V. It's found that the input referred noise in the proposed circuit is more compared to reference circuits. But this input referred noise does not affect much as the resolution is improved in case of the proposed comparator, as the difference in inputs at the input terminals (VIP and VIN) measured during kickback was found to be larger than the state of the art work thus improves the resolution.

In Fig. 13 evaluation of kickback noise and resolution at kickback of Proposed Comparator can be observed. The maximum deviation of the voltage at the two inputs from the applied inputs is the kickback noise. It is found that the kickback noise is reduced by 28.7 mV from the Zhuang's comparator. The resolution is also improved as the difference in inputs VIP and VIN during kickback is increased from 6.3 mV in case of Zhuang's comparator to 21.66 mV in case of proposed comparator for an input differential voltage of 10 mV.

Fig. 14 shows the energy required per comparison at a frequency of operation equal to 0.5 GHz. It can be observed that the energy required reduces for increase in the differential voltage across the input pairs. The energy required per comparison is increased in the proposed designs as it has an extra pre-amplification stage also it dissipates static power in the first pre-amplification stage in the form of pre charge currents (IpreC Large, IpreC Little Less) shown in Fig. 4 (a).

Variation of delay with respect to the differential input voltage is shown in Fig. 15. The delay in comparators is checked for 90 % settling of the output and it's observed that for an input differential voltage of 1 mV the delay observed is 433.4 ps, 346.3 ps, 336.9 ps, 333.6 ps, 181.7 ps, in Miyahara's [6], Elzakker's [7], Brandolini's [8], Zhuang's [10], Proposed Comparator respectively.

VI. CONCLUSION

This paper proposes four-stage comparator which has improved speed, kickback noise and resolution compared to the state-of-the-art works. The simulation result analysis shows that this comparator is suitable for high-speed, high resolution ADCs as it has improved resolution compared to the state-of-the-art works. The delay is reduced by 151.9 ps and 153.1 ps for OUTP and OUTN respectively proposed comparator from Zhuang's comparator.

Kickback noise is reduced by 28.7 mV and 36.1 mV for VIP and VIN respectively for the proposed design compared to Zhuang's design and also the difference in inputs VIP and VIN during kickback is increased from 6.3 mV for Zhuang's to 21.66 mV for proposed design at an input differential voltage of 10 mV thus it reduces effect of input referred noise on resolution as discussed in Section V.

There are certain limitations in the proposed work static power dissipation is there in the reset or pre-charge phase at the first stage of PMOS input pair through paths TP3-TP1-TN1 and TP3-TP2-TN2 shown in Fig. 4 (a), also the area of the circuit is more compared to state of the art works. There is scope for reduction in the size of circuit as well as the Energy required per comparison.

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