SEHS: Solar Energy Harvesting System for IoT Edge Node Devices

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Abstract. In IoT (internet of things) realm, sensors need an uninterrupted power supply for continuous operation. This paper presents an on chip solar EHS (SEHS) design for IoT edge node devices. For matching the impedance between solar cell and converter CVM technique is adopted. The energy efficient Hill-Climbing Algorithm (HCA) is adopted to follow the maximum power point (MPP). The control section takes care of the MPPT procedure, and computational load along with charging of the supercapacitor. LDO (low dropout regulators) is used to generate various voltages needed by the sensors. The proposed system is capable of providing power supply to various edge node devices in IoT. The SEHS is designed in CMOS 180nm technology. The output voltage is in the range of 1.2 V to 3.55 V with an input of 1-1.5 V. The SEHS is consuming 25μW of power, which is within the ultra-low power range in IoT.

Keywords: LDO · Maximum Power Point Tracking (MPPT) · Solar Energy Harvesting System (SEHS) · Capacitor Value Modulation (CVM) · IOTs.

1 INTRODUCTION

Recent developments in fabrication technology lead to use of tiny devices in IoT for numerous applications. Every aspect of life is now inspired by internet of things (IoT) and by 2020 the number of users is likely to exceed beyond 30 billion [23]. The IoT [12] consists of edge node devices at the bottom, gateways at the middle and cloud at the top as depicted in Fig. 1 (a). The edge node devices are mainly responsible for sensing, processing and communication, satisfying the properties of a smart node [12],[13]. The failure of these edge node devices leads to a catastrophic situation due to unavailability of power. In this paper, the

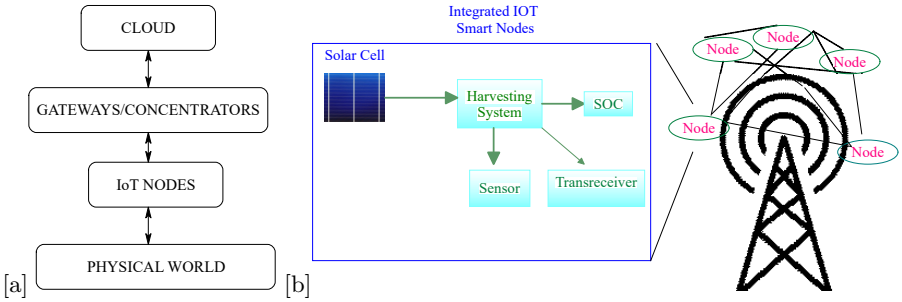


Fig. 1. (a) Different layers in IoT (b) An IoT Smart node

harnessing of natural resources is discussed towards designing a self- sustainable solar energy harvesting system (SEHS).

Towards a environment friendly approach for powering IoT devices, natural energy harvesting techniques should be adopted [12, 13, 11].There are various environmental friendly natural energy sources available such as Solar [10, 9], Thermo-electric generators (TEG) [3, 4], Radio-frequency (RF) [21], Microbial [7], and Wind [1]. The solar energy is found to be economic and suitable for IoT applications due to definite advantages like wide availability and no mechanical part involvement in the conversion process to electrical energy (direct current). By using appropriate MPPT algorithm, maximum power can be extracted [20]. The voltage generated by the small solar cell in IoT scenario may not be enough to drive the computational load and charge the supercapacitor [19]. Towards monolithic implementation switched converters circuits called as charge pumps(CP) are used [18]. The IoT smart node consists of an energy source, harvesting system, SOC, sensors and trans-receivers as depicted in Fig. 1 (b).

In this paper, section 1 is the introduction. Section 2 presents related work carried out by various researchers. Section 3 investigates the proposed solar harvesting system. Section 4 interprets low drop out regulators for load regulation. Section 5 validates the experimental setup and we conclude in Section 6.

2 RELATED WORK

Many researchers have discussed various natural energy resources like solar, microbial, RF, TEG, wind [1] and its usage towards energy harvesting [23][13]. Omairi et al. have presented control techniques to extract the maximum output from these sources in [13]. Shao et al. in [20] and Avalur et al. in [2] presented about the parameters that affect the solar cell behavior. The output achieved using the natural energy sources are low enough to drive the loads. Huynh et al. in [6] discussed about different voltage boosting techniques for converting low level voltage. Converters are used to boost the low voltages as discussed in [23, 11, 4, 18]. The current sensor is used for MPPT process and is well described in [3].

In [5] authors have presented the multiple voltage generation using low dropout regulators (LDOs). Ram et al. in [16, 17] discussed about the digital controller design using FSM (finite state machine) to control a specific operation.

The literature review and their results motivate us towards designing a monolithic solar EHS for powering the IoT edge node devices.The solar energy is widely accepted by research community as a viable alternative among the other available natural resources. The CVM technique in the MPPT process is used to match the impedance between the photo voltaic cell and the CP. The HCA is used for MPPT due to ease in hardware implementation. The combination of a boost, bulk and LDO regulates the loads at the output. The boost converter is implemented using CP as a voltage tripler. The contributions of this paper are (a) Design of a self-sustainable ultra-low power solar energy harvesting system (SEHS). (b) use of charge pumps as a boost converter and LDO being used that provides multiple power supplies with load regulation.

3 PROPOSED SOLAR ENERGY HARVESTING SYSTEM (SEHS)

Fig. 2 depicts the proposed solar EHS (SEHS).The main functionality of SEHS is to provide supply voltage to the IoT edge node devices and charging the supercapacitor/rechargeable battery. The CP used as a converter to boost the low input solar voltage and LDO at the load side to generate different voltages for the sensors. The control section monitors the total operation of the SEHS, which includes the control signals needed for operation of current sensor, MPPT procedure, recharging of the supercapacitor. The control section is implemented using finite state machine (FSM) as a digital controller. The proposed SEHS mainly consists of the following modules as clock and bias generation, CP as a voltage tripler, current sensor,MPPT module and LDO.

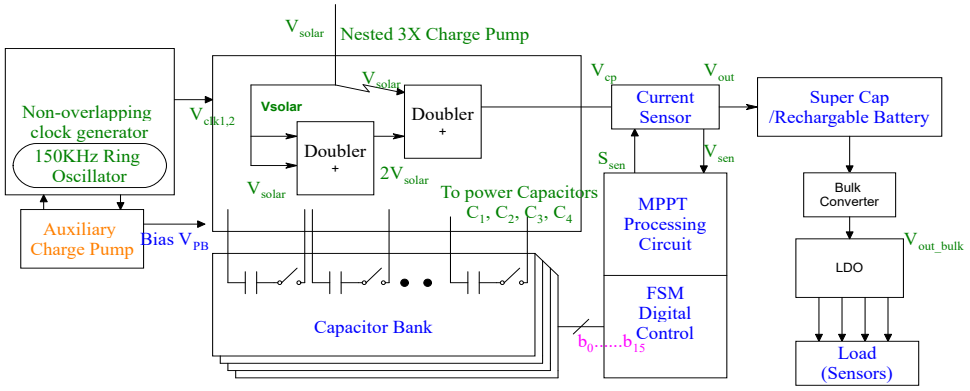


Fig. 2. Proposed Solar Energy Harvesting System

Clock and Bias Generation

The CMOS ring oscillator used in the design to generate the essential clock frequency of 150 kHz.This clock frequency is given to the non-overlapping clock generator (NOCG), which generates two non-overlapping clocks used by the auxiliary CP. The generation of higher bias voltages required for biasing the voltage tripler is provided by the auxiliary CP and higher clock amplitudes for tripler is generated by level shifters. Higher clock amplitudes help in reducing losses during charge transfer in converters.

Charge Pump as Voltage Tripler

The circuit diagram of the CP as a booster is shown in Fig. 3. The boosted output is achieved by applying the alternative clock pulses (V_{clk1} and V_{clk2}) to the CP across the capacitors C_u (includes C_1, C_2, C_3, C_4) and level up the negative plate by the same potential. Cascaded stages of two doubler are used as a tripler to provide a required supply to the nodes. The CP has a conversion ratio of three (CR=3). The MOSFETS MN_1 and MN_2 in Fig. 3 are driven separately with higher bias voltages to overcome lower turn on voltage with reduction in conduction resistance.

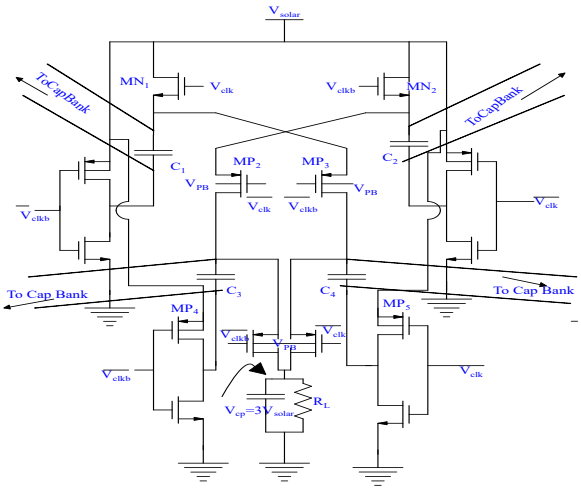


Fig. 3. CP as a Voltage Booster (Tripler)

The Z_{cp} (impedance of the boost converter) is described by [12]

$$Z_{cp} = \frac{V_{solar}}{I_{in}} = \frac{1}{2f_s C_u} \frac{1+\alpha}{\left(3 - \frac{V_{out}}{V_{solar}}\right)\alpha} \tag{1}$$

V_{solar} is the solar voltage, I_{in} is the input current of the charge pump (CP), f_s is the switching frequency, C_u is the pumping capacitor of CP, α is the capacitor ratio between the stages of the converter, V_{out} is the converter output. From

equation 1, it indicates that the impedance of the converter is inversely proportional to C_u. The capacitor C_u is connected with the digital capacitor bank for CVM to achieve impedance matching.From the analysis of small signal model of a tripler, it can be observed as

$$[2V_{solar} - (V_{out} - V_{solar})] \times \alpha C_u = \frac{1}{2} \times \frac{T \times V_{out}}{R_L} \tag{2}$$

where T is the switching period and R_L is load of the SOC.By rearranging equation 2 it can be written as

$$V_{solar} = \left(\frac{1}{2} * \frac{T}{R_L} * \frac{1}{\alpha C_u} + 1\right) * \frac{1}{3} * V_{out} \underrightarrow{Match} V_{MPP} \tag{3}$$

Equation 3 clarifies that, the MPPT can be achieved by tuning the clock frequency and the capacitor C_u. The tuning of frequency needs additional hardware, so in our design the frequency is made constant and capacitor value is varied using CVM. The CVM is done through digital capacitor banks. The digital capacitor banks consume less power with reduced noise. The CP is categorized on the basis of the power conversion efficiency (PCE) and is given by equation 4 as,

$$PCE = \frac{V_{out}}{V_{solar} \times CR} \times 100\% \tag{4}$$

A current sensor is employed to sense the response of the converter, when MPPT is needed. The control signal S_{sen} controls the total operation of the current sensor. The current sensor gets the desired biasing from the supercapacitor during MPPT process. The hill-climbing algorithm is implemented using CVM [8],[15]. The MPPT procedure with appropriate circuitry and required control signals from FSM for MPPT are depicted in Fig. 4(a).

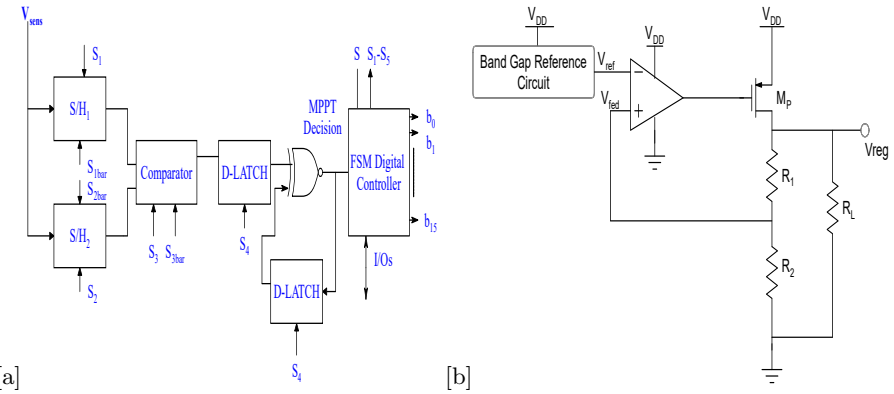


Fig. 4. (a) MPPT procedure with FSM Control Signal (b) Low Drop-out Regulator

4 LOW DROP-OUT REGULATORS (LDOs)

LDOs are simple circuits used to regulate an output response, that is fed from a higher input voltage. The load current is determined by size of the pass transistor (PT). The accuracy of LDO is determined by the open loop gain of error amplifier (EA). The stability of LDO should be assured to satisfy all load conditions. There is always a need to generate low level supply voltages (basically 1.2V-1.6V) from supercapacitor with best system efficiency. Different regulated voltages are generated by varying component resistor R_2. By varying load resistor R_L, it is expected that the designed LDO will give constant voltage irrespective of load variation. The basic circuit diagram of LDO is depicted in Fig. 4(b).

Pass Transistor

The supply voltage is applied to all the parts of circuitry as shown in Fig. 4(b). Regulated output can be taken from drain terminal of PT. The PMOS PT is used instead of NMOS due to the fact that, PMOS provides lower dropout voltage compared to NMOS PT. But the disadvantage with PMOS PT is that it provides higher output impedance.For NMOS pass transistor $V_{in}(\min)$ is given by

$$V_{in}(\min) = V_0 + V_{ds(sat)} + V_{gs} \tag{5}$$

V_0 is the output voltage, $V_{ds(sat)}$ is the drain to source saturation voltage and V_{gs} is the gate to source voltage. The output impedance $R_o = r_{ds}$ (ac drain resistance). For PMOS pass transistor $V_{in}(\min)$ is given by

$$V_{in}(\min) = V_{sg} + V_{ds(sat)} \tag{6}$$

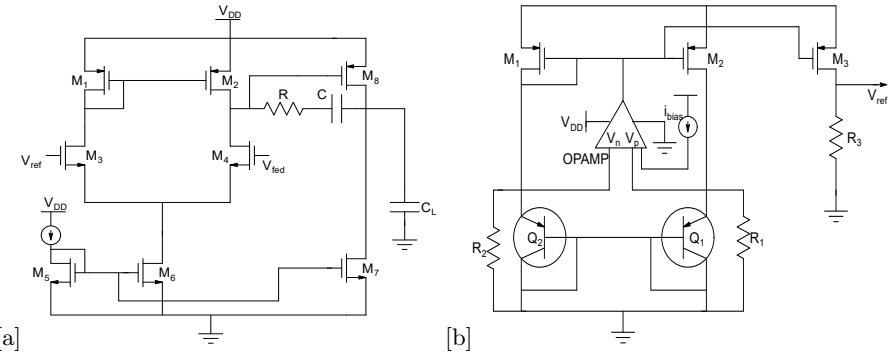


Fig. 5. (a) Error Amplifier (b) Band Gap Voltage Generator

Where $R_o = 1/g_m$.The g_m is the trans conductance. PMOS PT is used in this design to make sure that dropout voltage remain less. During the time when

loading increases at the output, more drain current is drawn through PT M_P; M_P drops more voltage across it. To compensate it, the gate to source voltage is reduced using EA and vice-versa.

Error Amplifier

The error amplifier is used to refer the output voltage using band-gap voltage reference (V_{ref}) input at one end of differential amplifier and output (V_{fed}) at other end.To improve stability, series combination of R and C is placed in between drain of M_2, M_4 and gate of PMOS M_8 to make two pole amplifier as depicted in Fig. 5(a). MOSFET M_5 and M_6 works as current mirror to provide same current in both branches. MOSFET M_7 is with larger W/L ratio for high current requirement at output stage, which is a common source amplifier. MOSFETs M_1, M_2, M_3 and M_4 acts as differential amplifier with differential input and single ended output with high CMRR, slew rate and moderate gain as shown in Fig. 5(b). To improve the gain such as to make amplifier more accurate, the second stage is included as MOSFET M_8 and M_P (pass transistor), so the overall gain will be very high, i.e. multiplication of gain of both stages.

Band gap Voltage Reference(BGR)

To provide a voltage reference (V_{ref}) to the error amplifier, a constant voltage independent of process(P), temperature(T), and supply voltage(V) is generated. The schematic of BGR circuit is shown in Fig. 5(b).It generates a constant voltage of 0.9 V to provide reference to one end of error amplifier.The diode connected BJTs Q_1 and Q_2 together with resistor R_1 acts as proportional to absolute temperature (PTAT) current generator, since difference voltage VD_2 -VD_1 is a function of thermal voltage (V_T) and the V_T has positive temperature coefficient (0.086mV/°C).The PTAP current in Fig. 5(b) is defined as

$$IPTAT = V_T * \frac{\ln K}{R_0} \tag{7}$$

The current flowing through the resistors, R_2 is complementary to absolute temperature (CTAT) since the voltage accross diode (VD_0) has a -ve temperature coefficient (-1.5mV/°C). The CTAT current in Fig. 5(b) is defined as

$$CTAT = \frac{V_{D_0}}{R_2} \tag{8}$$

MOSFETs M_1, M_2 and M_3 in Fig. 5(a) acts as current source to provide same current through all branches.By varying the value of resistor R_3 we can get different reference voltages.

5 EXPERIMENTAL SETUP

The self-sustainable solar energy harvesting system (SEHS) is designed in CMOS 180nm technology library. The capacitors in charge pumps and the digital capacitor banks (CBs) are metal-insulator-metal (MIM) type. The input voltage is in the range of 1-1.5 V. The load is characterized by using different value of resistors and the supercapacitor is characterized with a 33 mF value.

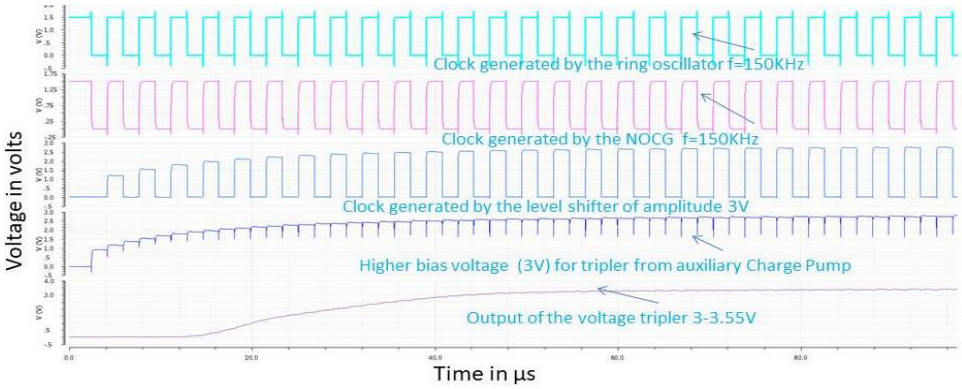


Fig. 6. Clocks and Bias generation using RO, NOCG, ACP, LS for tripler

5.1 Results and Discussion

SEHS Simulation with MPPT:

The signals like clocks, higher bias voltage, and boosted clock signal for voltage tripler for self-sustainable operation of the SEHS is depicted in Fig. 6. Once the MPPT is initiated, When the V_{solar} gets degraded, an environmental sensor S gets triggered and the MPPT process gets initiated. The control signals generated by FSM controller are S_1, S_2, S_3, S_4, S_5, b_0 to b_{15} etc. is depicted in Fig. 7. In Fig. 7, it depicts that till 150 μs, S is low indicating no MPPT. When S is high after 150 μs, MPPT process is triggered. When S_{sen} is high the current is sensed as V_{sen} at the output of current sensor.The S_1 and S_2 are high for 14-clcok cycles each to sense the old and new power information. In between S_1 and S_2 the CVM is done, using the binary to thermometer codes b_0 to b_{15}, which is initially high and becomes low one by one at each MPPT cycle for CVM as depicted in Fig. 7. The S_3 and S_4 are high at appropriate time to take the final decision of MPPT achievement in 30^{th} and 31^{st} clock cycles and are shown in Fig. 7. The comparator output is initially high (V_{out_comp}= 1) and when the new power is more than the old power, V_{out_comp} is zero as shown in Fig. 7 by first black circle. This makes the X_{nor_out} to be zero (which is initially high) by second black circle indicating the achievement of MPPT and is shown in Fig. 7. This leads to reset all the control signals and the SEHS continue to charge the supercapacitor.The simulation result in Fig. 7 confirms that once the MPP is achieved the MPP is locked. In our experimental analysis after two number of MPPT cycle the MPP occurs. The input voltage is in between 1-1.5 V and output of the tripler is 3-3.55 V. A bulk converter is used generate the 1.8 V from the supercapacitor such that it is used by the LDO to handle loads of different voltage levels.

Low Drop-out Regulator

The LDO designed is suitable for sensors used in consumer electronic devices and IoTs with a voltage requirement of 1.2 V-1.8 V. The input voltage to LDO

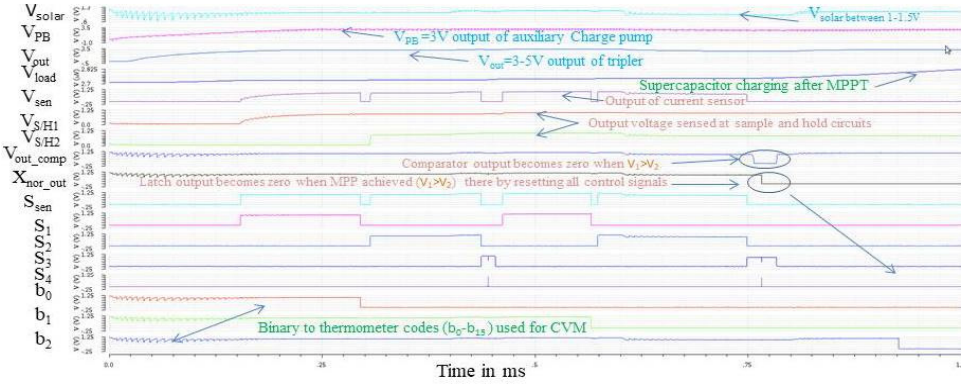


Fig. 7. SEHS Complete Simulation (with MPPT achievement) with control signals

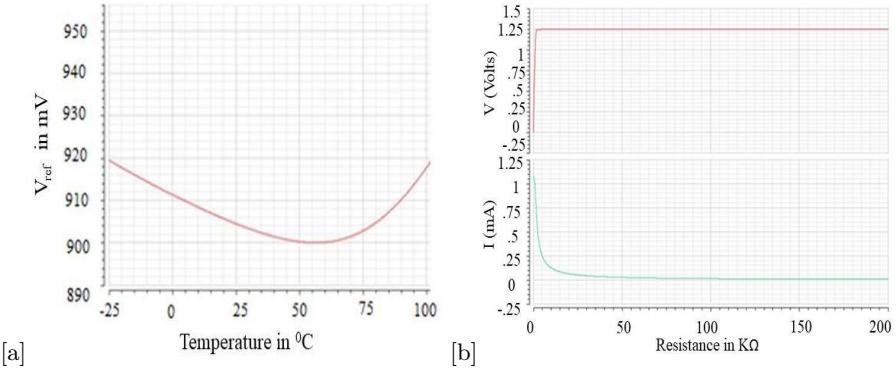


Fig. 8. (a) Reference Voltage v/s Temperature (b) Output Voltage v/s Output Resistance with Resistor R_2=80k

is from buck converter and is 1.8 V. Fig. 8(a) shows the variation of reference voltage with variations of temperature which closely constant at 0.9 V.

Low Dropout Voltage with Load Variations:

Ideally regulated voltage should be constant irrespective of load variation. As shown in Fig. 8(b) for feedback resistors R_1=30 kΩ and R_2=80 kΩ (in Fig. 4(b)) which provides the constant voltage of approximately 1.25V for range of load variation. The regulated voltage is optimum until the load current of 0.5 mA.

For feedback resistors R_1=30KΩ and R_2=40 kΩ, which provides the constant voltage of approximately 1.58 V for range of load variation as depicted in Fig. 9(a). The regulated voltage is optimum until load current of 0.31 mA.

Generation of Different Regulated Voltages using Resistor R_2:

As shown in Fig. 9(a), Fig. 9(b) the different voltages can be generated in the range from 1.2 V to 1.6 V using supply voltage of 1.8 V by controlling the resistor R_2.

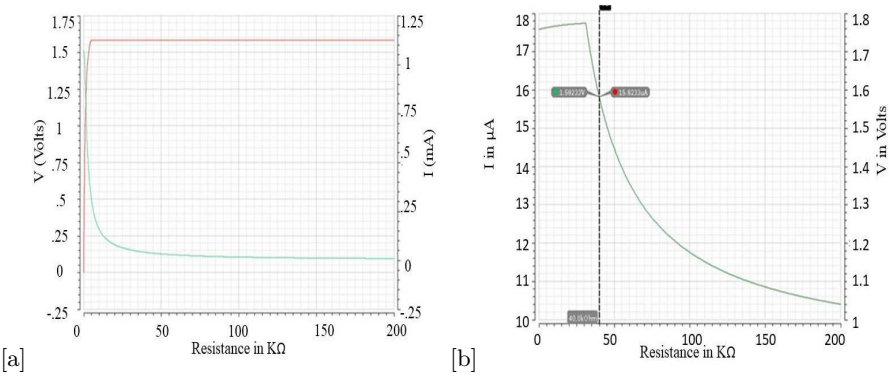
Hence Band-gap voltage reference and Error amplifier is designed to be used in low drop out regulator. Buffer circuits are used to do impedance matching and to generate different voltages for biasing MOSFET. Low drop out voltage regulator is designed with constant output voltages 1.2 V, 1.4 V and 1.6 V using 1.8 V input voltage irrespective of load variations.The comparison of different low energy solar harvesting system with proposed system is depicted in Table. 1.

6 CONCLUSION

The unavailability of power supply for the edge node devices in the IoT leads to a catastrophic situation and malfunctioning of devices. The state of art SEHS designed for powering the IoT sensors is a challenge and is well addressed in this paper. The SEHS is well suited for the input solar voltage in the range from 1-1.55 V and output achieved at the tripler output is 3-3.55 V. The LDO used in this design generates various supply voltages for IoT sensors with good power load regulation. The efficiency of the charge pump as a voltage tripler is 87 % to 97 % at different inputs in the range of 1-1.5 V. The entire SEHS is powered by the solar cell and no external bias is required. The higher bias voltage generated on-chip and the total SEHS is self-sustainable.

Table 1. Proposed work v/s different low energy solar harvesting systems

Reference	**[20]**	**[10]**	**[14]**	**[22]**	**[9]**	**[12]**	**Proposed work**
Technology	350nm	350nm	250nm	130nm	350nm	180nm	180nm
Fully Integrated	Yes	Yes	No	Yes	No	Yes	Yes
Self-sustaining	No	No	Yes	Yes	Yes	Yes	Yes
Input Range (V)	2.1-3.5	1-2.7	0.5-2	1.8	1.5-5	1-1.5	1-1.5
Output Range (V)	3.6-4.4	2	0-5	1.4	0-4	3-3.5	3-3.55
Power Throughput (μW)	100-775	0-80	5-1000	< 10	800	0-29	0-25
LDO for Load Regulation	No	No	No	No	No	No	Yes



[a] [b]

Fig. 9. (a) Output Voltage v/s Output Resistance with Resistor R_2=40k (b) Regulated Voltage v/s Feedback Resistor R_6

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