An Improved ZVS-PWM Buck Converter with ZCS Auxiliary Circuit

Manikant Kumar
Department of Electrical Engineering, NIT Rourkela, Rourkela, Odisha, India-769008
manikant6038@gmail.com

Monalisa Pattnaik
Department of Electrical Engineering, NIT Rourkela, Rourkela, Odisha, India-769008
pattnaikm@nitrkl.ac.in

Jyotismita Mishra
Department of Electrical Engineering, NIT Rourkela, Rourkela, Odisha, India-769008
jyotismita.mishra22@gmail.com

***Abstract*— This paper presents a soft switching technique to improve the efficiency of isolated and non-isolated power converters in the high-frequency range. The designed converter uses two switches i.e. main switch and auxiliary switch which are operated in Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) respectively. Here, different circuit modes of ZVS PWM buck converter with the proposed ZCS auxiliary circuit is analyzed. The operating principle is also discussed with generalized auxiliary circuit. The PWM pulse for main switch and auxiliary switch with desired delay has been generated using analog circuit. A 35 W, 200 kHz ZVS-ZCS buck converter is simulated in Matlab/Simulink environment and experimentally verified.**

Keywords— Zero Voltage Switching (ZVS), Zero Current Switching (ZCS), auxiliary circuit, buck converter

I. INTRODUCTION

Now a days, a huge demand for the smaller, lighter and efficient power converter has forced the researchers to work on high frequency [1]. This high frequency can be implemented with switching devices which can turn on and turn off at very high speed when power is being exchanged from input to output side. These switches are operated at high frequency to reduce the size of passive component like inductor, capacitor, transformer implemented during designing of the power converters. Working at high frequency is profitable. However, it leads to increase switching loss and hence the efficiency of the power converters reduces.

In [1], soft switching technique is used to reduce the switching losses. However, it may be damaged during voltage fluctuation and current stress across the switch. A novel zero voltage transition (ZVT) PWM converter proposed in [2] has minimum current and voltage stress. In [3], an active clamp circuit is proposed which works under ZVS for a complete family of PWM dc/dc converters. In this, all converters have the advantage of soft commutation with minimum voltage stress. Furthermore, ZVS in auxiliary circuit is discussed in [4], [5]. Here, stresses across switches is lower than those found in other power converters. But it has switching losses and handles less power than main power circuit, which is not desirable at high frequency. The family of active clamp circuit [6] has used coupled inductor in which the power converter is dependent upon the auxiliary circuit, which is not preferable. In [7], ZVT boost converter with an auxiliary circuit for improvement of power factor is presented. Here, current stress for switch is low due to zero resonant current.

Power converter introduced in [8] contains an auxiliary circuit which operates in such a way that auxiliary switch turns on in ZCS condition and main switch operates at ZVS. In this, its power circuit is isolated with auxilary circuit using coupled inductor. Moreover, the Auxiliary circuit can be implemented in all types of the isolated or non-isolated buck converter. In [9], soft switching current waveforms have lower electromagnetic interference (EMI). Here, passive elements have been realized for highly efficent solar energy battery charger with ZVS resonant converter.

A novel ZCS bi-directional buck, boost converter for rechargeable energy storage application has been discussed in [10] and [11]. Here, the conventional buck converter is upgraded with the implementation of auxiliary switch, which is forced in such a way that the switch turned-off under ZCS condition. Further, the piecewise linear model of the quasi-resonant converter [12] and its controlling technique is analyzed with state-space and averaging modeling.

In this paper, the proposed circuit is a soft switching buck converter which encounters all the problems mentioned above. Here, a capacitor is introduced to rectify the problem associated with mentioned literature which is the cause of non-isolation with the main power converter due to coupled inductor. Furthermore, a diode is introduced antiparallel to auxiliary MOSFET (M_a) to operate during reverse current across M_a. A capacitor is also introduced parallel to the main MOSFET (M_m) to work in ZVS. A unique analog circuit based pulse generation is introduced to drive main MOSFET as well as auxiliary MOSFET. The control strategy applied in proposed converter is such a way that the main switch operates in ZVS and the auxiliary switch turns on in ZCS condition.

The paper organization is as follows: section II presents modes of operation, mathematical analysis of the proposed converter. Section III deals with the parameter calculation of ZVS-ZCS buck converter which contains main and auxiliary circuit. Section IV represents the simulation of ZVS-ZCS buck converter. Experimental results are discussed in section V. Finally, the conclusion is presented in section VI.

II. CIRCUIT DESCRIPTION

Fig. 1 shows the basic switching circuit and V-I characteristics of power converter. In Fig. 1 (b) power dissipation during transition is shown. The active and passive switch present in the circuit is *S* and *D*. Here, the switch voltage and current are denoted as V_s and I_s respectively. It is seen that losses across switch at the time of transition is very high and makes the system inefficient [7].

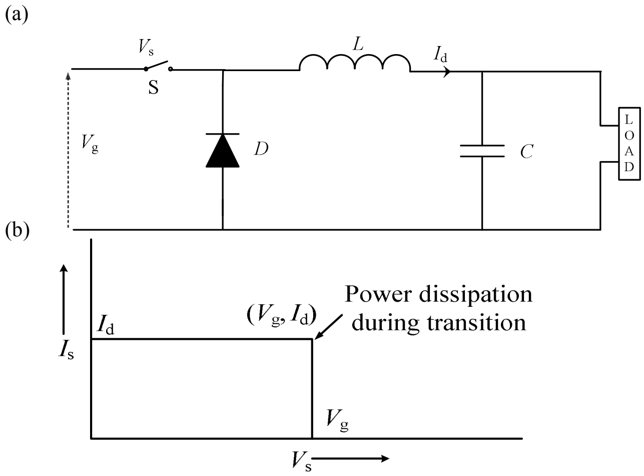


Fig. 1. (a) Basic circuit diagram of a converter, (b) switching characteristics

The designed buck converter with the auxiliary circuit is shown in Fig. 2. It consists of two sub circuits, one part of the circuit is main circuit while other circuit referred to as auxiliary circuit as shown by dotted line in Fig. 2. The main sub-circuit is conventional buck converter consists of a switch (MOSFET M_m), diode (D), filter inductor (L) and a capacitor (C) to reduce harmonics. On the other hand, auxiliary circuit consists of auxiliary MOSFET (M_a), L_r, C_r, D_{C1}, D_{C2}, D_{C3}. The proposed circuit is implemented to get ZVS across the main MOSFET and ZCS across auxiliary circuit.

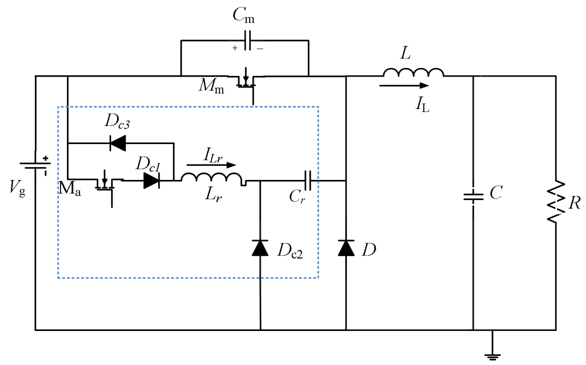


Fig. 2. Circuit diagram of proposed converter

The modes of operations are shown in Fig. 3 for different switching interval. The theoretical waveform of the proposed buck converter is shown in Fig. 4.

Mode 0 (interval $t < t_0$):

Before $t < t_0$, V_{cr} (voltage across the resonant capacitor) is constant and equal to V_g, and the equivalent circuit is shown in Fig. 3(a). In this mode main MOSFET (M_m) and auxiliary MOSFET (M_a) both are off. Moreover, load current flows through diode D. Hence load current and diode current is equal.

$$I_L = I_d \tag{1}$$

Mode 1 (Interval $t_0 < t < t_1$):

From Fig. 4, it is seen that when the auxiliary MOSFET turned on, the current flowing through the L-C circuit (resonant circuit) is sinusoidal. At $t = t_1$ the current flowing through the L-C circuit is equal to load current. At this instant, diode D is reversed biased and the current through the diode (I_d) is zero. Mode 1 equivalent circuit is shown in Fig 3(b). In this mode, voltage across the main switch is V_{cm} and capacitor present across it is charged up to the input voltage. Mathematical analysis is given as follows:

$$V_{Cm}(t) = V_g \tag{2}$$

$$V_{Cr}(t) = V_g(1-\cos\omega_1 t) \tag{3}$$

$$\omega_1 = \frac{1}{\sqrt{L_r C_r}} \tag{4}$$

$$I_{Lr}(t) = V_g\sqrt{\frac{C_r}{L_r}}\sin\omega_1 t \tag{5}$$

$$V_{Cm}(t) = V_g(1-\cos\omega_1 t) \tag{6}$$

Mode 2 (interval $t_1 < t < t_2$):

Equivalent circuit of mode 2 is shown in Fig. 3(c). Mode 2 starts when the diode current I_d is zero. Now, the current through C_m is equal to I_{Lr} - I_L. During this mode, voltage across C_m decreases with increment of voltage across C_r. This interval ends when V_{cm} is zero.

$$I_{Lr}(t) = V_g\sqrt{\frac{C_m \parallel C_r}{L}}\cos(\omega_1 T_1)\sin\omega_2 t + I_L\cos\omega_2 t \tag{7}$$

$$\omega_2 = \frac{1}{\sqrt{L(C_m \parallel C_r)}} \tag{8}$$

As $C_m << C_r$ above equation can be rewritten (considering approximation)

Now,

$$V_{Cm}(t) = V_g(1-\cos\omega_1 T_1) + V_g\cos(\omega_1 T_1)\cos\omega_2 t - I_L\sqrt{\frac{L_r}{C_m}}\sin\omega_2 t \tag{9}$$

$$V_{Cm}(t) = V_g(1-\cos\omega_1 T_1) = V_{Cr} \tag{10}$$

Mode 3 (interval $t_2 < t < t_3$)

The mode 3 equivalent circuit is shown in Fig. 3(d). In this mode, current flows through the body diode of the main switch. MOSFET is switched on when voltage across M_m is zero and hence ZVS is achieved.

Mode 4 (interval $t_3 < t < t_4$);

The equivalent circuit of mode 4 is shown in Fig 3(e). At $t = t_3$, circuit enters into mode 4. It ends when auxiliary current is zero. As the current through auxiliary is zero, M_a is switched off which leads to ZCS. The equation governing for mode 3 and 4 are same and given in Equation (11).

$$I_{Lr}(t) = V_{Cr}(T_1)\sqrt{\frac{C_r}{L_r}}\sin\omega_1 t + I_{Lr}(T_2)\cos\omega_1 t \qquad (11)$$

Mode 5 (interval $t_4 < t < t_5$)

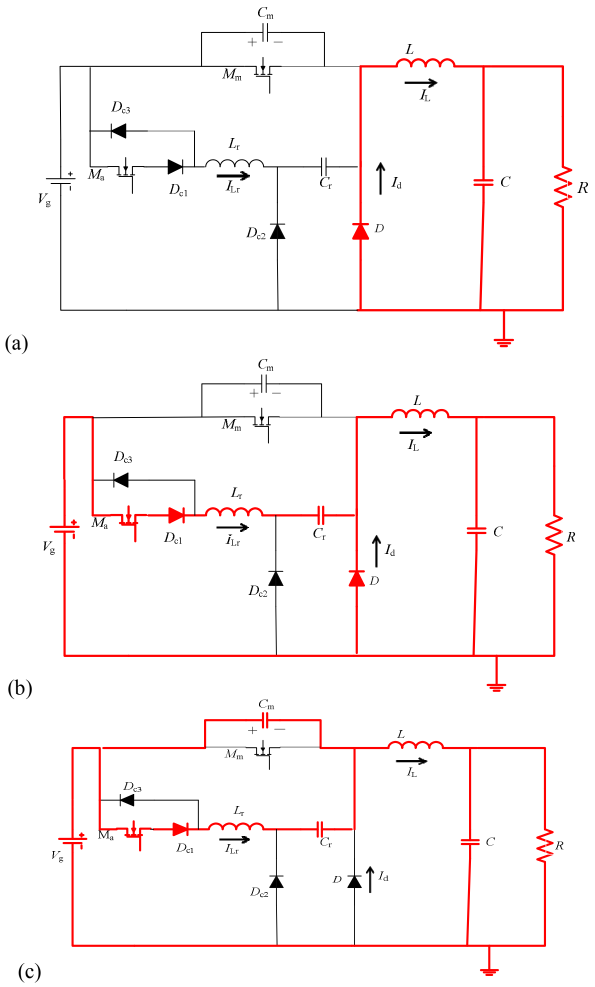
Mode 5 starts at t_4. In this mode, current flows through D_{c3}. The voltage across C_m starts decreasing as shown in Fig. 3 and diode D also conducts. Load current I_L flows through inductor L.

Mode 6 (interval $t_5 < t < t_6$)

The circuit diagram of mode 6 is shown in Fig. 3(g). In this mode, the main switch is on, and the auxiliary switch is off. The steady state operation of buck converter starts after t_5. Load current I_L is flowing through load R. This is normal operation of ZVS buck converter

Mode 7 (interval $t_6 < t < t_7$)

The equivalent circuit of mode 7 is shown in Fig 3(h). This mode starts when M_m is turned off, and D_{c2} begins to conduct. Also, the load current is the summation of the current across C_r and C_m. Hence, during this interval the main switch is turned off in ZVS condition. Now load current starts flowing through diode D, and again mode 0 starts.



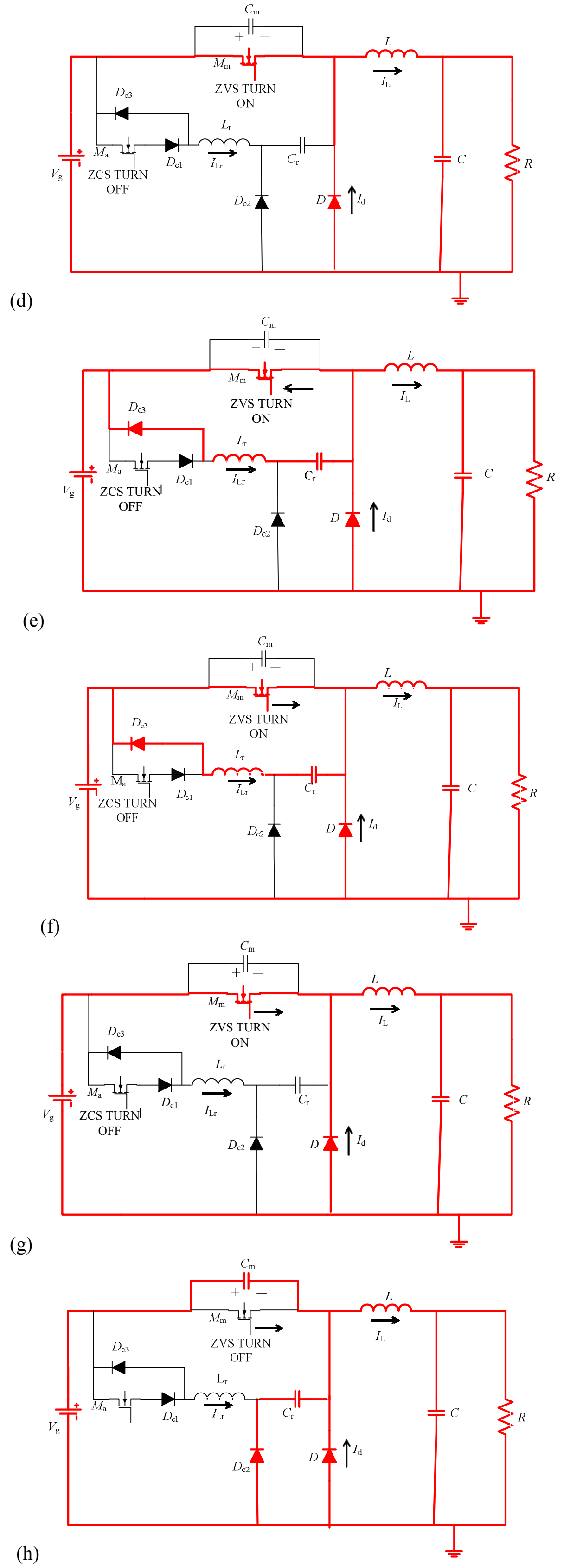


Fig. 3. Equivalent circuit for (a) mode 0, (b) mode 1, (c) mode 2, (d) mode 3, (e) mode 4, (f) mode 5, (g) mode 6, (h) mode7

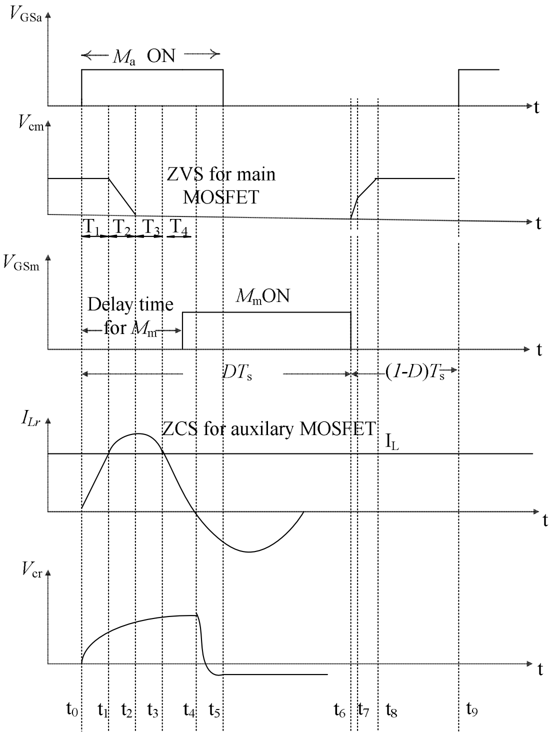


Fig. 4. Theoretical waveform of proposed converter

III. Design Procedure of Proposed Converter

The procedure for selection of buck converter components are same as conventional hard switching power converter [7].

Design of resonant inductor (L_r) and resonant capacitor (C_r): The resonant inductor and resonant capacitor together decides the rise time of the auxiliary circuit. Significant rise time leads to power loss during turn on. Similarly, fall time should be less. The larger value of L_r is the cause of significant increase of rise time whereas the circuit requirement is to shorten the resonant interval.

As the *L-C* circuit gives resonant frequency and it will be very high, so length of the resonant interval is approximately quarter of the resonant period [7] as shown in Equation (12).

$$t_r = \frac{\pi\sqrt{L_r C_r}}{2} \tag{12}$$

So L_r and C_r selection is based on maximum value of turn-on time (5 to 10%). As L_r is calculated from Equation (12), the value of C_r is decided in medium range because lower value of C_r increases voltage stress across the main switch and larger value of C_r enhances the peak of auxiliary current [7]. C_r is calculated from Equation (13).

$$C_r = \frac{It_f}{2V} \tag{13}$$

where I is on state current, V is off state voltage, t_f is fall time of the main switch.

Selection of auxiliary switch (M_a) and Diode (D_{c1}), (D_{c2}), (D_{c3}): A capacitor connected in circuit influences operation in the high-frequency range. The selection of switch is made on the basis of rising time, fall time and delay of the switch. There must be less reverse recovery time for the high-frequency operation.

Gating signal for the Main switch and Auxiliary switch: Timing diagram to generate driving pulses for proposed converter is given in Fig. 5. Delay pulse can be generated using 74LS123. Block diagram of pulse generation with delay circuit is presented in Fig. 6. To operate the main switch, M_m in ZVS and M_a in ZCS, the turn on of auxiliary MOSFET must be greater than $t = T_1 + T_2 + T_3$ as shown in Fig. 3. It ensures the turn on of the M_a and it is at zero current which leads to ZCS. The operation of the main MOSFET in ZVS can be achieved when switch is turn on after a delay of more than $t = T_1 + T_2$ as shown is Fig.5.

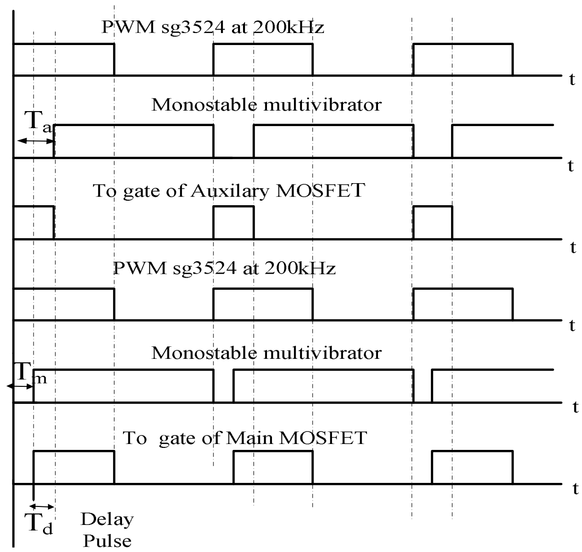


Fig. 5. Main MOSFET and Auxiliary MOSFET duty cycle control strategy.

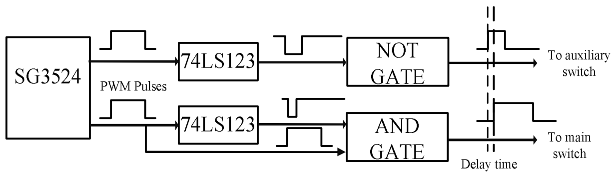


Fig. 6. Block diagram of pulse generation with delay circuit

IV. Simulation Results And Discussions

Simulation of ZVS-ZCS buck converter is done in MATLAB/Simulink environment by considering circuit parameter given in Table I. Here, design of each component is calculated using nonideal condition. A 38W, 200 kHz ZCS-ZVS buck converter is simulated and results are shown in Fig. 7, Fig. 8 and Fig. 9.

TABLE I. COMPONENTS USED FOR SIMULATION OF BUCK CONVERTER

Parameters	Value
Input voltage (V_g)	24V
Output voltage (V_o)	12.6 V
Output power (P_o)	38W
Inductor (L)	45uH
Capacitor (C)	100uF
Load resistance (R)	3.2 Ohm
Frequency (f)	200kHz
Resonant inductor (L_r)	0.4uH
Resonant capacitor (C_r)	100nF
Capacitor (C_m)	4.7nF

Fig.7 shows the delay pulse waveforms to drive both the MOSFET. A delay of 0.6 µs is generated to prevent from short circuiting.

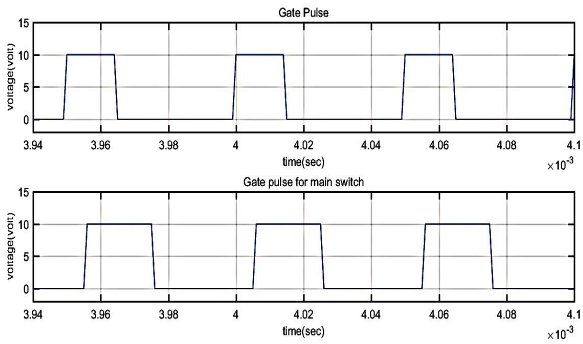


Fig. 7. Gate pulse for main and auxiliary MOSFET with a delay of 0.6 µs at 200 kHz

Fig. 8 shows the gate pulse for ZVS for M_m and the switch voltage across M_m. As the voltage across the main MOSFET is zero during turn on, the condition of ZVS is achieved.

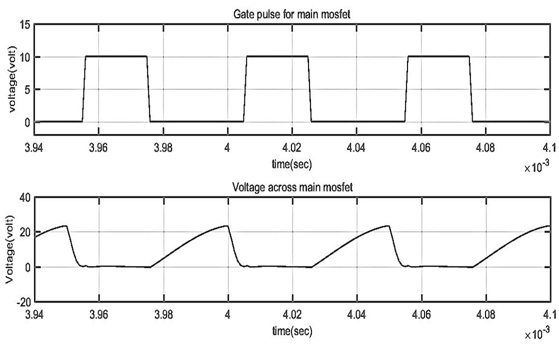


Fig. 8. Gate pulse and drain to source voltage across main MOSFET

The gate pulse and the current flowing through the auxiliary MOSFET is shown in Fig. 9. The auxiliary switch is turned off when current flowing through the MOSFET is zero. As there is no overlapping of the voltage across the switch and the current flowing through it, there is no switching loss.

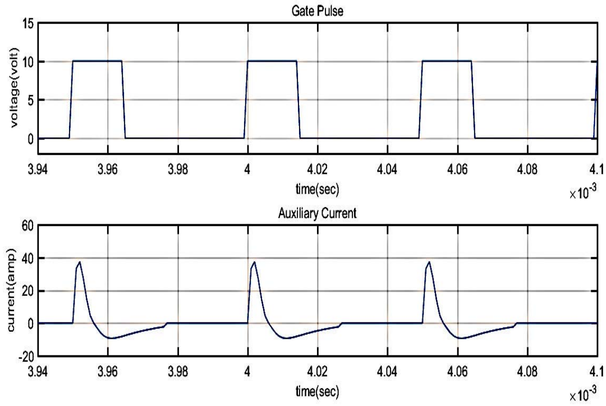


Fig. 9. Gate pulse and current flowing through the auxiliary MOSFET

V. EXPERIMENTAL RESULTS AND DISCUSSIONS

Experimental setup is shown in Fig. 10. In this, IRF 740 is used as both main and auxiliary MOSFET. SG3524 is used to generate 200 kHz pulse. Then a delay circuit is designed using 74LS123 monostable multivibrator. A prototype of 35W, 200 kHz ZVS-ZCS buck converter is developed in laboratory.

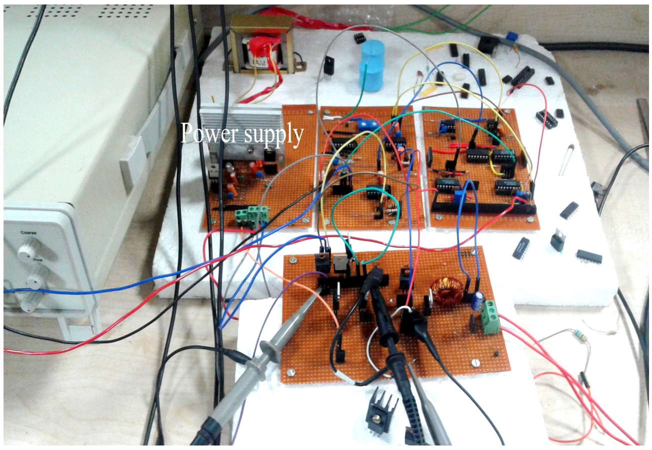


Fig. 10. Experimental setup

TABLE II. COMPONENTS USED FOR IMPLEMENTATION OF BUCK CONVERTER

Parameters	Values
Input voltage (V_g)	24V
Output voltage (V_0)	11.2 V
Output power (P_o)	35W
Voltage ripple (V_r)	1%
Current ripple (I_r)	30%
Inductor (L)	80uH
Capacitor (C)	100uF
Load resistance (R)	3.8 Ohm
Frequency (f)	200kHz
Resonant inductor (L_r)	1uH
Resonant capacitor (C_r)	100nF
Capacitor (C_m)	4.7nF

A 200 kHz of gate pulses for main and auxiliary MOSFET is shown in Fig. 11(a). In this figure, 0.6 µs of delay is generated to prevent short circuit. Fig. 11 (b) shows the waveform of gate pulse of main MOSFET and the switch voltage across it. The gate pulse drives the switch when switch voltage is zero. Therefore, the condition of ZVS is achieved. Fig. 11 (c) shows the drain to source voltage and current thorough auxiliary MOSFET. The encircled path shows that when current is zero, the auxiliary switch is turned-off at ZCS. As ZVS and ZCS are achieved for both main and auxiliary switch, the switching losses are zero. The measured efficiency of the converter is 86%.

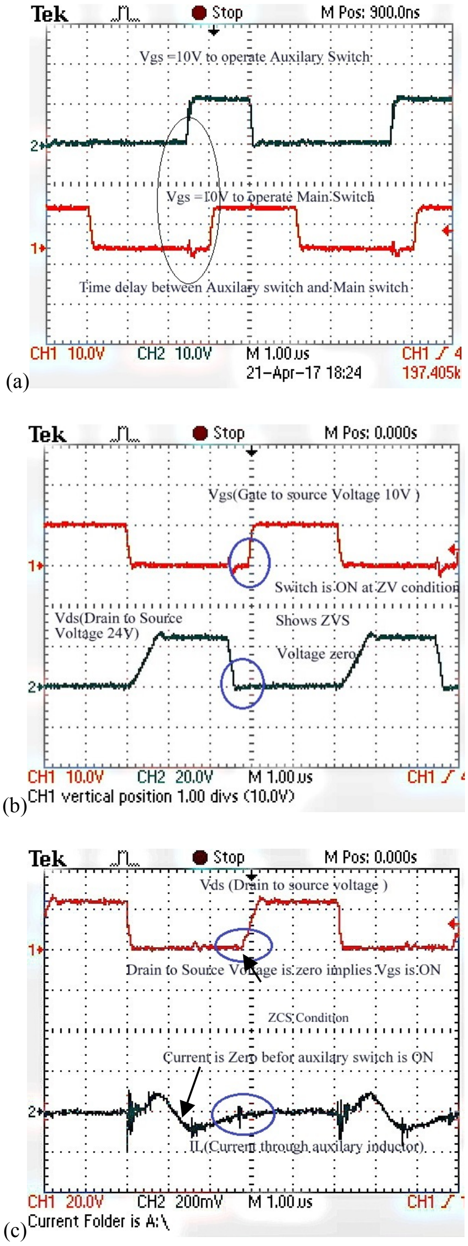


Fig. 11. Experimental waveforms of ZVS-ZCS buck converter (a) gate pulse for M_a and M_m, (b) V_{gs} and V_{DS} of main MOSFET (c) V_{ds} and current through auxiliary MOSFET

VI. CONCLUSION

A ZVS-ZCS based DC-DC buck converter with auxiliary circuit has been proposed in this paper. The proposed auxiliary circuit can be implemented in each isolated or non-isolated converter i.e. buck, boost, buck-boost, SEPIC, forward etc. The capacitor C_{r2} is introduced to isolate the auxiliary circuit from the main circuit. The initial design of converter is same as conventional converters. However, selection of resonant inductor and capacitor depends upon the rise and fall time of auxiliary current and voltage. A 35 W, 200 kHz ZVS-ZCS buck converter is designed and implemented. The measured steady state efficiency of the proposed converter is 86% which is more efficient as the switching losses across main and auxiliary MOSFET is zero.

REFERENCES

[1] R. W. De Doncker and J. P. Lyons, “The auxiliary resonant commutated pole converter,” in *Industry Applications Society Annual Meeting, 1990., Conference Record of the 1990 IEEE*, pp. 1228–1235, 1990.

[2] G. Hua, C.-S. Leu, Y. Jiang, and F. C. Y. Lee, “Novel zero-voltage-transition PWM converters,” *IEEE Trans. Power Electron.*, vol. 9, no. 2, pp. 213–219, 1994.

[3] C. M. C. Duarte and I. Barbi, “A family of ZVS-PWM active-clamping DC-to-DC converters: synthesis, analysis, design, and experimentation,” *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 44, no. 8, pp. 698–704, 1997.

[4] G. Moschopoulos, P. K. Jain, Y.-F. Liu, and G. Joos, “A zero-voltage-switched PWM boost converter with an energy feedforward auxiliary circuit,” *IEEE Trans. Power Electron.*, vol. 14, no. 4, pp. 653–662, 1999.

[5] S. Chattopadhyay, S. Baratam, and H. Agrawal, “A new family of active clamp PWM dc-dc converters with ZVS for main switch and ZCS for auxiliary switch,” in *Applied Power Electronics Conference and Exposition (APEC), Twenty-Sixth Annual IEEE*, 2011, pp. 851–858, 2011.

[6] N. Lakshminarasamma, B. Swaminathan, and V. Ramanarayanan, “A unified model for the ZVS DC-DC converters with active clamp,” in *Power Electronics Specialists Conference, 2004. PESC 04. IEEE 35th Annual*, 2004, vol. 3, pp. 2441–2447, 2004.

[7] N. Jain, P. K. Jain, and G. Joós, “A zero voltage transition boost converter employing a soft switching auxiliary circuit with reduced conduction losses,” *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 130–139, 2004.

[8] N. Lakshminarasamma and V. Ramanarayanan, “A family of auxiliary switch ZVS-PWM DC-DC converters with coupled inductor,” in *IECON Proceedings (Industrial Electronics Conference)*, pp. 2660–2665, 2006,.

[9] Y.-C. Chuang and Y.-L. Ke, “A novel high-efficiency battery charger with a buck zero-voltage-switching resonant converter,” *IEEE Trans. Energy Convers.*, vol. 22, no. 4, pp. 848–854, 2007.

[10] V. V. S. K. Bhajana and P. Drabek, “A novel ZCS bidirectional buck-boost DC-DC converters for energy storage applications,” in *Conference on Industrial Technology (ICIT), 2015 IEEE International*, pp. 872–877, 2015.

[11] Y. Xi and P. K. Jain, “A forward converter topology employing a resonant auxiliary circuit to achieve soft switching and power transformer resetting,” *IEEE Trans. Ind. Electron.*, vol. 50, no. 1, pp. 132–140, 2003.

[12] A. Nejadpak and F. Tahami, “Stabilizing controller design for quasi-resonant converters described by a class of piecewise linear models,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 61, no. 1, pp. 312–323, 2014.