

RF and Noise performance exploration of Double Gate FinFET

K. P. Pradhan, P. K Sahu.

Abstract- Double Gate FinFET devices are suitable for nano electronic circuits due to better scalability, higher on-current (I_{on}), improved Sub-threshold Slope (SS) and undoped body (no random dopant fluctuation). Body thickness (T_{si}) increases the gate control over the channel resulting in reduced short channel effects (SCEs). Thin T_{si} increases the quantum confinement of charge, resulting increased threshold-voltage (V_{th}), and hence, reduced performance. In this work, we have varied the process parameters like channel length (L_g) in presence of noise and analyzed various parameters. Significant variation in the noise spectral density has been observed, which is related to the random occurrence of excess Lorentzian components ($1/f^2$ -like nature) associated with generation-recombination (GR) noise.

Keywords- Double Gate FinFET, Sub-threshold Slope (SS), short channel effects (SCEs), Quantum confinement, noise spectral density.

I. Introduction

Noise is a spontaneous fluctuation in current or in voltage, which is generated in all semiconductor devices. The intensity of these voltage fluctuations or current fluctuations depend on device type, its manufacturing process, and operating conditions. The resulted noise is the combination of different noise sources, which is called as an inherent noise. The inherent noise can also be used as the quality assessment of semiconductor devices. Often it has been used as an important factor during the development of the production process of new semiconductor devices. The important sources of noise are thermal noise, shot noise, generation-recombination noise, $1/f$ noise (flicker noise), $1/f^2$ noise, burst noise or random telegraph signal (RTS) noise and avalanche noise etc.[1][2]. In general, the analysis of the noise performance of the transistors is critical for developing low-noise applications with a reduced cost.

SOI devices are suitable candidates to become an alternative to conventional bulk CMOS. Advanced MOSFET structures such as ultra-thin-body silicon-on-insulator (SOI) single-gate and double-gate (DG) transistors can be scaled more aggressively than the bulk Si structures; hence, it can be adapted for IC production. A fully depleted double gate (DG) silicon-on-insulator (SOI) is called as a near ideal technology, which gives a higher drive current than its single gate (SG) counterpart due to larger control over channel region that further enhances the immunity towards short channel effects (SCEs) and provides an almost ideal sub-threshold slope [3].

In this paper, the Small signal and RF noise properties of Double Gate FinFET is discussed at the theoretical point of view. The present work also describes the variation in the noise spectral density over different bias voltages and process parameters.

II. Device Structure

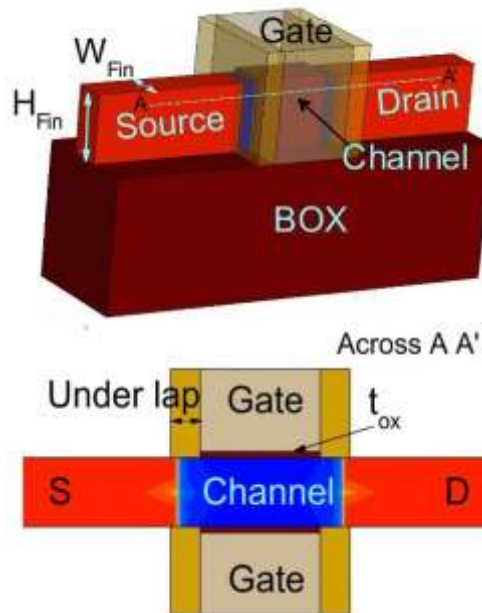


Fig.1 3-D and 2-D cross sectional view of the simulated device

TABLE I. DEVICE PARAMETERS USED IN THE TCAD SIMULATION OBTAINED FROM ITRS 2013

Design	HP	LOP	LSTP	This Work DG-MOSFET
L_g (nm)	20	20	20	50nm to 20nm
T_{Si} (nm)	5	5	5	15nm to 5nm
EOT(nm)	0.84	0.9	1.2	1.1nm
V_{DD} (V)	0.85	0.67	0.87	0.7V

III. Simulation Setup

The simulated device (Fig.1) consists of DG-FinFET operating with a power supply voltage of $V_{DD} = 0.7$ V. Source/channel and channel/drain junctions are considered to be abrupt with continuous doping of $1 \times 10^{15} \text{ cm}^{-3}$ in channel region [4]. Different noise power spectral density plots have been analyzed with variation in bias voltages and process parameters. The work function of the metal gates is fixed at 4.5 eV to achieve the desired V_{th} value. The drift-diffusion model is used as the default carrier transport model in Sentaurus device simulator [5], which is activated in the simulation. The basic mobility model is used to consider the effect of doping dependence, high-field saturation (velocity saturation), and transverse field dependence. The impact ionization effects are ignored in our device simulation. The Poisson equation, continuity equations, and the different thermal and energy equations are solved self consistently to provide accurate results in the simulation.

IV. Result and Discussion

A typical behavior of the drain current noise spectral density (S_{id}) versus drain current (I_D), channel length (L_g) and gate to source voltage (V_{GS}) in DG FinFET devices are represented in Fig.2 for a measurement frequency (f) of 1MHz.

A. With L_g variation

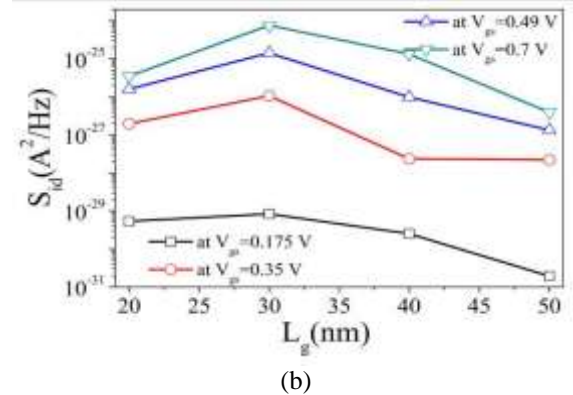
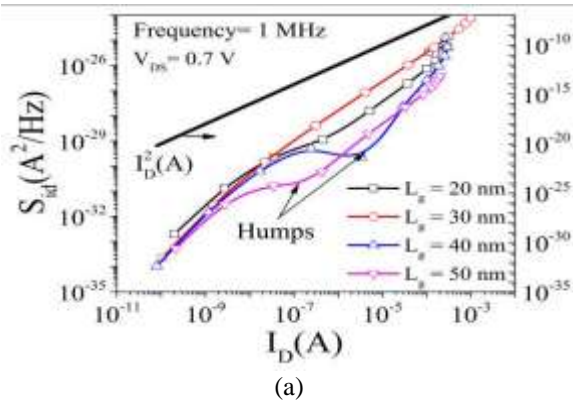
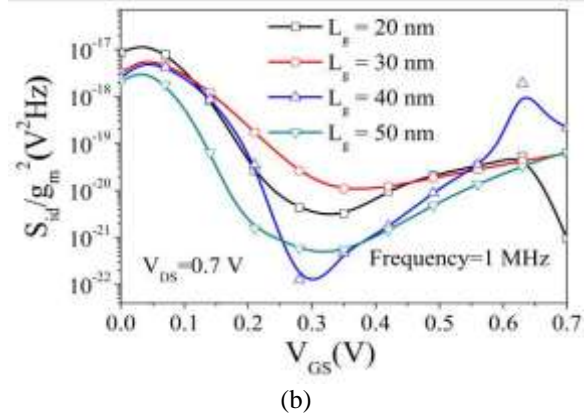
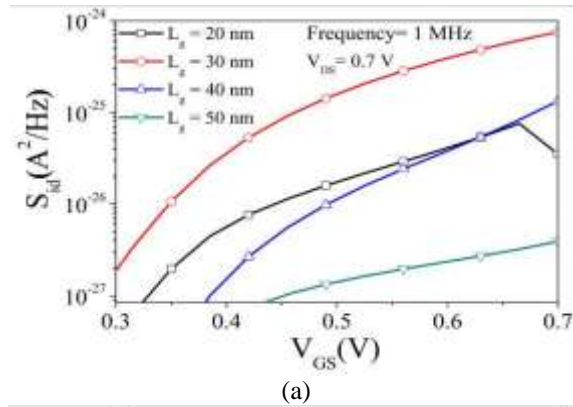
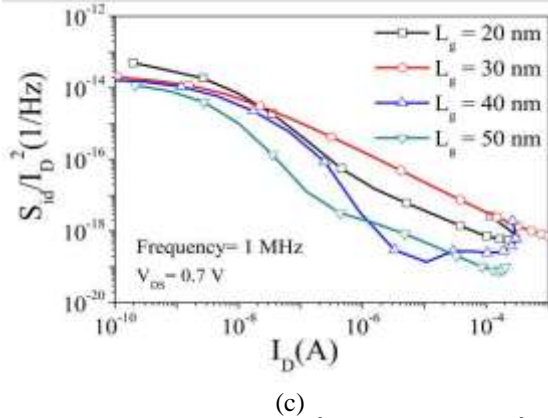


Fig.2 (a) S_{id} vs. I_D for different gate lengths (L_g), (b) S_{id} for different L_g with variation in V_{GS}

From Fig.2 (a), it is observed that S_{id} follows the quadratic law for low drain currents. The dependency of S_{id} on channel length is represented in Fig.2 (b), where S_{id} is plotted for n-MOS devices with channel length of $L_g = 20, 30, 40, 50$ nm respectively for different V_{GS} , at $V_{DS} = 0.7$ V and $f = 1$ MHz. It can also be identified from Fig.2 (b) that the value of noise spectral density is more for higher L_g ($L_g = 50$ nm) and a gradually decrement is observed for lower L_g values. Here the model predicts a significant decrement in S_{id} at low gate biases, particularly for the longer channel devices.





(c)
 Fig.3 (a) S_{id} vs. V_{GS} , (b) S_{id}/g_m^2 vs. V_{GS} , (c) S_{id}/I_D^2 vs. I_D , with variation in channel length (L_g)

S_{id} , S_{id}/g_m^2 , and S_{id}/I_D^2 are examined in Fig.3 (a), (b), and (c) respectively. Without the inclusion of SCEs (for higher L_g devices), the PSD of drain noise current is significantly underestimated. From Fig.3 (b), it is observed that the value of S_{id}/g_m^2 increases for lower L_g ($L_g = 20$ nm) due to mobility fluctuations (mobility model is used in the simulation). With the increase in drain current, the value of S_{id}/I_D^2 decreases which is explained in Fig.3 (c). It is also observed from the Fig.3 (c) that the value of S_{id}/I_D^2 is high for lower value of L_g ($L_g = 20$ nm) and low for higher value of L_g ($L_g = 50$ nm).

V. Conclusion

In this paper, the analysis of noise is made by considering the S_{id} , S_{id}/g_m^2 , and S_{id}/I_D^2 results. The variation of structural parameters such as L_g , and T_{Si} are considered on noise power spectral densities. This work provides a simulation study of the high frequency noise in 2D devices with different channel lengths, and silicon thickness. It is observed that with an increase in channel thickness, the volume inversion increases due to electro-static integrity which increases the current, resulting an increase in noise power spectral density.

References

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