FPGA Prototyping and Parameterised based Resource Evaluation of Network on Chip Architecture

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***Abstract*—This paper investigates the various aspects of network on Chip(NoC) design and its FPGA implementation. A parametric approach of evaluating the FPGA resources, delay and maximum frequency of operation for a NoC design has been described which may help the designer to take early decision related to NoC designing and prototyping. Virtual channel(VC), flit buffer depth and flit data width are taken as the parameter for evaluation. The functional simulation results show a successful data transfer between different nodes of a 3x3 NoC. Increase in VCs increases the FPGA resources, delay and reduces the frequency of operation. The maximum frequency of operation is also affected by the variation of Flit Data Width and Flit Buffer Depth.**

Keywords—NoC, Mesh, Router, FPGA,Parametric Evaluation

I. INTRODUCTION

The ever increasing demand in portable and smart computing brought electronics design to a new paradigm where a large number of electronics components can be integrated into a single chip called System on Chip (SoC). SoC integrates different cores such as processor, memory, input, output peripheral cores. Other cores such as GPU, radios and bridges are also integrated into a single chip. SoC finds applications in variety of domains such as aerospace, military and medical sciences and cellular technology. The integration of large number of cores comes with additional challenges like core-to-core communication, energy efficient design along with increased computing performance of the SoC[1].

SoCs are traditionally employ shared bus architecture for communicating between different cores. But this provides certain limitation such as reduced bandwidth along with not scalable architecture. In order to deal with this challenges and increase communication between high density components, Network on Chip (NoC) has been proposed. NoC is a subset of SoC, that comprises of different nodes connected via routers, Network interfaces (NIs) are used to connect core to routers in a network. The various parts of NoCs are routers, NIs, links, switches, buffers, allocators and virtual channels. The communication between the cores occurs by sending the packets through the network. A packet comprises of flow control digits (flits). Routing algorithms are used to provide path for the packets for transmission within a network from source node to destination node [2][3].

Many efforts have been noticed in literatures, to model and evaluate the performance of NoCs. Mathematically NoCs are modeled and simulations are carried out to evaluate the performance of the NoC. All these simulations are dependent on assumptions which limits their accuracy to some level. Hence hardware implementations using applications specific ICs and FPGAs are used to create the prototype to model the NoC in physical level. In comparison to ASICs, FPGAs offer less implementation cost and more design flexibility [4].

Kundu et al. [5] has proposed a new topology named mesh of tree (MOT) and evaluates its performance in comparison with other existing topology such as butterfly fat-tree topology.

Abba et al. [6] presented a parametric method to evaluate the performance of NoCs in FPGAs. FPGA implementation has been done for three NoC topologies mesh, torus and fat-tree, using CONNECT [7] generated Verilog cores. They have observed that flit data width(FDW) and flit buffer depth(FBD) impacts the FPGA resources. Hence various performance metrics of NoCs under both simulator and FPGAs has been carried out to assist engineers to take early decisions in relate to choosing of NoC performance parameters.

Arjomand et al. [4] has proposed a prototype model of NoC to implement in FPGA for multimedia applications.

Most of the papers have been presenting the NoC performance evaluation in both simulator or FPGA level. But few paper presents the final implementation of the NoC in FPGA and its functional simulations. In this paper various aspects of implementation of a 3x3 NoC in FPGA has been described.

The main contributions of this paper is as follow:

- A Router is modeled in hardware description language VHDL and functional validation of model ensures the accuracy of the router model.
- Design of 3x3 NoC in FPGA and validating its functionality using Xilinx ISE Software[].
- A parametric based evaluation is carried out in FPGA for 3x3 NoCs to observe the utilization of resources under selected parameters.

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Section II gives a background idea on NoC and its different design explorations. The various FPGA prototype of NoC is highlighted in section III. Section IV discusses the experimental setup. Section V and VI discusses the simulation results and synthesis results of the NoC implementation. Finally, section VII concludes the work.

II. BACKGROUND

NoC enforces many design explorations. Such as network topology, routing algorithm and network flow control.

A. Topology

Topology defines how the routers are connected to each other in an on chip Network and how the data will be shared through routers. It is analogous to road map and represented as a graph. A topology decides the hop count to reach the destination, therefore it influences the latency. The common network topologies are Ring, Mesh, Torus etc. Among these Mesh is the mostly used topology and has been used in this paper for implementation.

2 D Mesh Topology

A 2 D mesh topology is simplest form of local interconnections among IPs. Moreover, the 2 D mesh routing is easy to implement, causing in small size, broad bandwidth, smaller clock cycle, and overall performance and scalability. Mesh is the mostly used topology because of dimension ordered and is well matched for the packaging constraints. The advantages of Mesh topology are it can be operating at high frequencies, if any one of the node in the mesh gets failed the data operation won't fail because there is an alternate path for each and every router and we can expand the number of nodes without disturbing other nodes. A mesh-shaped network consists of m columns and n rows. The routers are situated in the intersections of the two wires and the computational resources are near routers. Addresses of routers and resources can be easily defined as x-y coordinates in mesh. The regular mesh network is also called as Manhattan Street network [15].

B. Routing Methodologies

The routing algorithm is used to make decision on what path a message will take through traversing in the network from source node to its destination node. The goal of the routing algorithm is to intelligently distribute the traffic evenly in the network among the all possible paths supplied by the network topology, so as to avoid congestion, hotspots and reduce contention, thus improving network latency and throughput [8]. Routing algorithms are classified as deterministic, oblivious and adaptive routing algorithm. XY is the mostly used deterministic routing algorithm that uses X-direction first to route packets followed by Y-direction. It uses no virtual channel. Hence easy to implement. Many other routing algorithms are proposed such as turn model [9], odd-even [10] and dyad routing algorithm [11].

Adaptive routing uses the information about the faulty link that can be by passed and reached to the destination with adaptive properties of algorithm, hence improving the throughput of the system [8].

C. Flow Control Mechanism

Flow control superintend the allotment of network buffers and network links. It regulates when buffers and links are assigned to messages and the sets of data at which they are granted. A good flow control deals the anatomy experienced by messages. It involves in determining work energy and power utilization. when a message is inserted to the network, first it is separated into packets and then into fixed length flits. The packets consist head flit, body flit and tail flit. Again the flit can be broken down into Phits. Flow controls are categorized into circuit switching, virtual cut through, packet based, store-forward and wormhole flow control [8].

Basically wormhole flow control cut the flits and then allowing flits to going on to the next router, but before that it checks the entire packet is received the current position or location. For this the flits can depart the current point or node. It controls the allocates storage and band width, to flits then the entire packets. It allows the small flit buffers, which is to be used in each router and for large packet sizes also. When it uses buffers explicitly makes inefficient use of link band width. However, it allocates storage and band width in flit sized units. In this router a link is held for the duration of a packets lifetime. When a packet is blocked, all the physical links held by that packets are left lethargic or inactive [8].

III. FPGA PROTOTYPE OF NOC

This section describes the various aspects of FPGA implementation of NoC architecture. Fig. 1 shows a 3x3 mesh architecture, which consists of 3 rows, 3 columns and a sum total of 9 nodes. Each node consists of bidirectional router that connects to other routers and an IP core through network interface.

Network interface also handles the handshaking signal between router and each IP cores. Depending on the placement of router switch each router has different number of ports. As an example the corner router switch has 3 ports whereas the central switch has 5 no.s of ports.

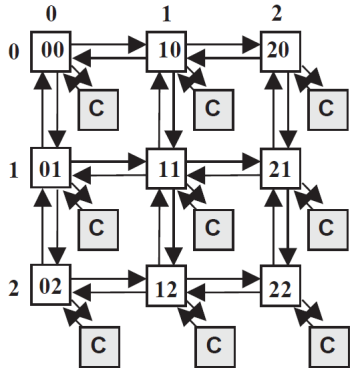

Fig. 1 A 3x3 mesh network [12]

The router is designed using Hermes switch [12] and ATLAS environment [13].

A. *Hermes Router*

Hermes architecture based router is used in this work to prototype NoC. Routers are used to transfer messages between IP cores. Fig. 2 shows, Hermes switch architecture comprises of routing control logic, five bidirectional ports. These are north, south, east and west. An input buffer is used in each port for storage of information. The ports are used to communicate with neighbor routers, whereas local port is used to communicate with the local IP core. These communication ports have buffer in input and output channels that can be used for temporary storage of information.

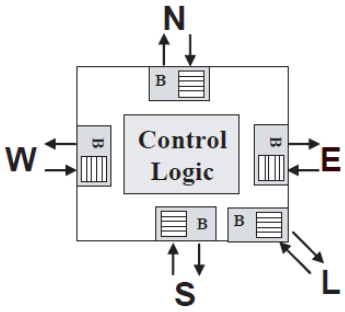

Fig. 2 Hermes Router [12]

As wormhole switching provides low latency and requires less memory, this is adapted as the switching methodology in the router architecture. In wormhole routing, packets are divided into flits. So the flits are parameterized so that it can be changed according to the requirement of application. Packets consists of header flit, that contains the address of the destination. The simplified XY routing algorithm is used to provide path for packets to reach the destination node. An arbitration module is used in the control logic that grants the incoming packets to execute XY routing algorithm to reach destination node [12].

IV. Experimental Setup

Hermes router is implemented in FPGA and verified for its functional validation. The 3x3 network is designed and implemented in Virtex-7, XC7VH290t FPGA board and the hardware resources are observed. Xilinx ISE 14.3[14] is used to write and simulate the VHDL code of the NoC.

The synthesis results such as slice, slice FF count and frequency of operations are noted. Three router parameters are varied and each set of VHDL code is synthesized to observe the hardware resources and frequency of operation.

The parameters are:

virtual channel: No. of virtual channel (VC) is changed from 1-4 and hardware resources are observed. Increase in VC increases the slice count of the NoC design.

Flit Data Width(FDW): FDW is defined in bits and has a significant impact on slice count and frequency of operation.

Flit Buffer Depth (FBD): FBD is define in terms of flits. Deeper buffer offers better performance by allowing packets to make more progress under heavy load [5]. FDW and FBD are changed to values 4,8,16,32 and 8,16,32 respectively to observe the FPGA resource utilization and frequency of operations.

V. Functional Simulation

A. *Simulation of Router*

In this simulation test of the Router, we have given the data at the Local (represents 3), so in order to receive the input we have to enable the receive control signal of local i.e. rx (4) and since we are using 2 VCs for each port, we have to represent in which VC we are giving data for that lane_ra(4). Credit signal represents weather the buffer has space to store the Flits.

In this the first flit “f5 (11110101)” represents the header flit, here we have taken the present router node as 0(0,0), from the header the destination address node is 3(1,1). Therefore, the direction of the flit traversal is in the East (0) direction, we can observe in the wave form of the data out [0]. The “tx” control signal represents the transmitting of data, in this router transmitting data in the East direction so it enables the tx(0) signal. Immediate next to the header is counter flit represents the number of flits contains in the payload also we can say body flits including tail flit. In this the number of payload flits are 8, so after transmitting 8 flits, after counter flit it became 0 as shown in Fig. 3.

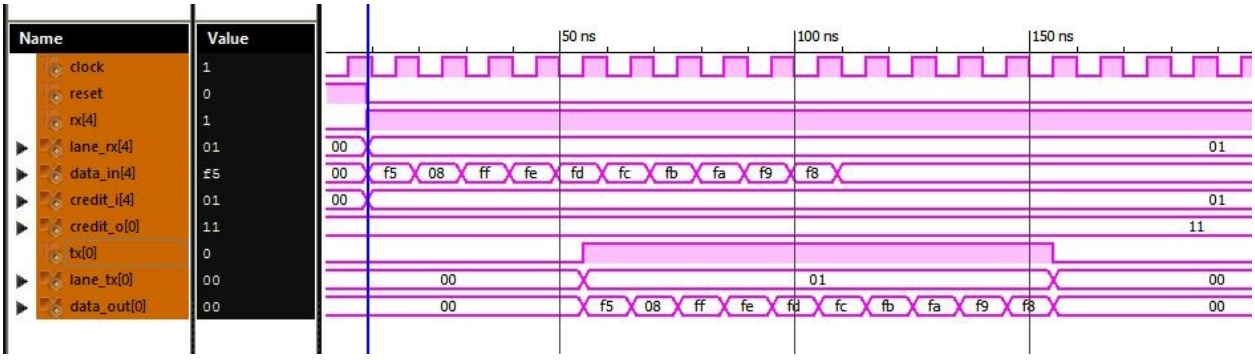

Fig. 3 Simulation result of 5 port router having 2 VCs, Flit width=8 and Buffer Depth=16

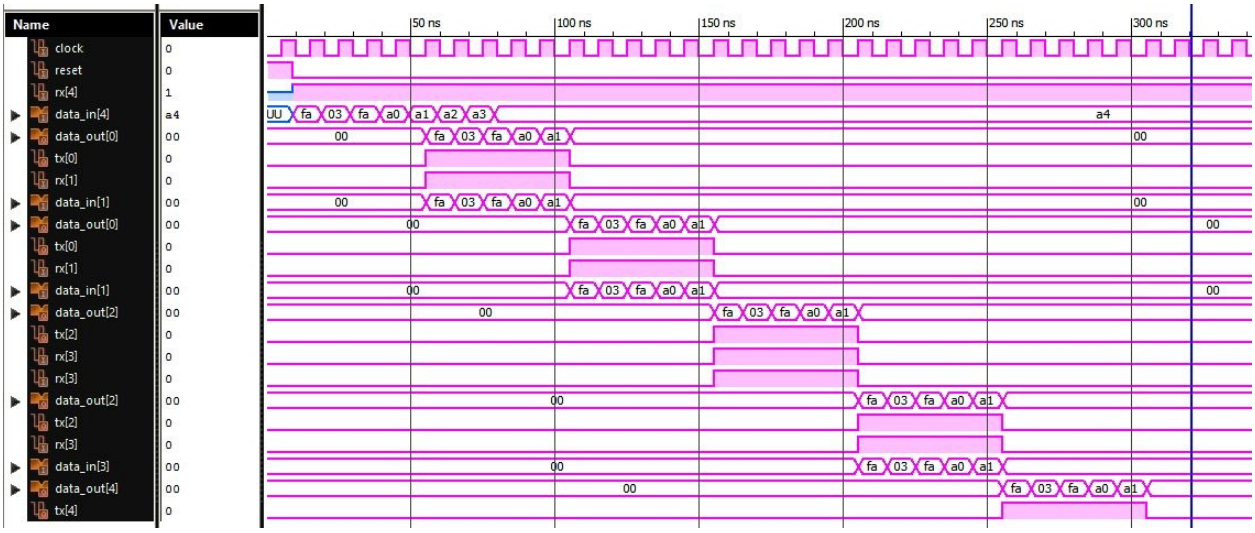

Fig. 4 Fuctional Simulation results of 3X3 NoC

B. Simulation results of 3x3 NoC

In this NoC 3X3 test simulation, we have given input at the router 0 through Local, at this node the destination X address dx is greater than present router address px so the router will transfer the data in the direction East and the flits reaches the Node 1 as shown in Fig. 4. At Node 1 the router 1 compares the X addresses and transfer the data in the East direction. After reaching the flits Node 2 the router compares X addresses of present and destination since both are equal it will compare Y addresses of present and destination since destination Y address is greater than present it will transfer in the direction North. At the Node 5 it will select North direction, At the Node 8 both X and Y address are same means the flits reaches destination and router sends the flits into Local.

TABLE I. COMPARISON OF AREA, FREQUENCY AND DELAY FOR THE 3X3 NOC WITH DIFFERENT VCS AND BUFFER DEPTH BY KEEPING FLIT WIDTH CONSTANT=8

VC	Buffer Depth	Area(slices)	Max. Frequency (MHz)	Max. combinational path delay(ns)
1	4	2690	149.988	0.339
	8	2758	149.988	0.339
	16	2922	149.988	0.339
	32	2977	149.988	0.339
2	4	6459	154.407	2.406
	8	6421	155.863	2.883
	16	6885	155.082	2.883
	32	7279	155.082	2.883
4	4	15045	119.610	3.319
	8	14966	118.902	3.319
	16	15972	118.902	3.319
	32	16736	118.902	3.319

VI. PARAMETERISE SYNTHESIS RESULT

Table 1 shows the synthesis results of 3x3 NoC in Xilinx ISE[14] that shows the variation in area and max frequency of operation and combinational delay. Here VC is changed from 1,2 and 4. FBD takes a parametric value of 4,8,16 and 32. Each table shows the results for variable FDW of 8,16, and 32.

TABLE II. COMPARISON OF AREA, FREQUENCY AND DELAY FOR THE 3X3 NOC WITH DIFFERENT VCS AND BUFFER DEPTH BY KEEPING FLIT WIDTH CONSTANT=16

VC	Buffer Depth	Area(slices)	Max. Frequency (MHz)	Max. combinational path delay(ns)
1	4	3936	139.523	0.339
	8	4000	139.523	0.339
	16	4189	139.523	0.339
	32	4256	139.523	0.339
2	4	8665	142.739	2.924
	8	8795	143.016	2.924
	16	10180	141.912	2.924
	32	10377	141.912	2.924
4	4	19633	117.123	3.567
	8	19964	117.123	3.567
	16	22440	117.102	3.567
	32	22802	117.102	3.567

TABLE III. COMPARISON OF AREA, FREQUENCY AND DELAY FOR THE 3X3 NOC WITH DIFFERENT VCS AND BUFFER DEPTH BY Keeping Flit width constant=32

VC	Buffer Depth	Area(slices)	Max. Frequency (MHz)	Max. combinational path delay(ns)
1	4	6301	126.875	0.339
	8	6366	126.875	0.339
	16	6565	126.875	0.339
	32	6631	126.875	0.339
2	4	13260	129.11	2.452
	8	13389	128.18	2.452
	16	14779	131.685	2.452
	32	14976	131.685	2.452
4	4	28427	109.417	3.244
	8	28724	109.404	3.244
	16	31083	109.377	3.244
	32	31503	109.377	3.244

VII. CONCLUSIONS

This paper uses the Hermes router switch and design a 3x3 2D mesh NoC. The functional simulation of router and NoC depicts that the design is working correctly. The parameterized synthesis results of the FPGA implementation of the NoC is presented. Three parameters chosen are VC, FDW and FBD. The results depict that increase in no. VC increases the FPGA area in terms of no. of slices. Increase in VCs increases the delay and reduces the frequency of operation. The maximum frequency of operation is also affected by the increase in FDW and FBD.

Finally, the parameterized methodology employed in this paper may assist designer to maintain a database and take timely decisions about different geometry of architectures and its variation in terms of hardware resources and frequency of operation.

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