

Threshold Voltage Modeling of Recessed - Source/drain Soi Mosfets with Vertical Gaussian Doping Profile

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Abstract: Recessed-source/drain (Re-S/D) SOI MOSFETs are being researched in both academia and industry because of its high drain current drive capability [1-2]. Fully depleted Re-S/D SOI MOSFETs possess superior short channel immunity and near ideal subthreshold characteristics. In a Re-S/D SOI MOSFET, source and drain are extended deeper into the buried oxide (BOX) in order to decrease the series resistance. A number of attempts have been made to model the subthreshold characteristics of Re-S/D SOI MOSFETs with undoped and uniformly doped channel for getting more physical insight [1-3]. However, the actual doping profile after the ion implantation step differs from uniform profile and resembles much with the Gaussian profile [4]. In addition, the Gaussian profile in turn gives two more parameters, projected range (R_p) and straggle (σ_p), which can control the device characteristics.

In the present work, an attempt has been made to model the threshold voltage of Re-S/D SOI MOSFETs with vertical Gaussian doping profile in the channel. The two dimensional (2D) Poisson's equation has been solved in the channel region of the device considering the appropriate boundary conditions. We have adopted the so called "virtual cathode approach" for the threshold voltage modeling. The developed analytical model predicts the threshold voltage of the device for wide variations in the device parameters. To verify the accuracy of the present analytical model, the model results are compared by ATLASTM device simulator [5].

[1] G.K. Saramekala, Abirmoya Santra, Sarvesh Dubey, Satyabrata Jit, Pramod Kumar Tiwari, "An analytical threshold voltage model for a short-channel dual-metal-gate (DMG) recessed-source/drain (Re-S/D) SOI MOSFET", Superlattices and Microstructures 60 (2013), pp. 580–595.

[2] Ajit Kumar, Pramod Kumar Tiwari, "A threshold voltage model of short-channel fully-depleted recessed-source/drain (Re-S/D) UTB SOI MOSFETs including substrate induced surface potential effects", Solid-State Electronics 95 (2014), pp. 52–60.

[3] B. Svilicic, V. Jovanovic, T. Suligoj, "Analytical models of front- and back-gate potential distribution and threshold voltage for recessed source/drain UTB SOI MOSFETs", Solid-State Electronics 53 (2009), pp. 540–547.

[4] Guohe Zhang, Zhibiao Shao, Kai Zhou, "Threshold Voltage Model of Short-Channel FD-SOI MOSFETs With Vertical Gaussian Profile", IEEE Trans. Electron Devices, vol. 55, no. 3, March 2008, pp. 803-809

[5] ATLAS User's Manual, Silvaco International, Santa Clara, CA, 2012.

Acknowledgment

The present work is supported by the project number SERC/ET-0415/2012.



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In the present work, an attempt has been made to model the threshold voltage of Re-S/D SOI MOSFETs with vertical Gaussian doping profile in the channel. The two dimensional (2D) Poisson's equation has been solved in the channel region of the device considering the appropriate boundary conditions. We have adopted the so called "virtual cathode approach" for the threshold voltage modeling. The developed analytical model predicts the threshold voltage of the device for wide variations in the device parameters. To verify the accuracy of the present analytical model, the model results are compared by ATLAS™ device simulator.

Outline

- Introduction
- Device Structure
- Analytical Modeling of Re-S/D SOI MOSFETs
- Results and Discussion
- Conclusion
- References

Introduction

Recessed-source/drain (Re-S/D) SOI MOSFETs are being researched in both academia and industry because of its high drain current drive capability [1-2]. Fully depleted Re-S/D SOI MOSFETs possess superior short channel immunity and near ideal subthreshold characteristics. In a Re-S/D SOI MOSFET, source and drain are extended deeper into the buried oxide (BOX) in order to decrease the series resistance. A number of attempts have been made to model the subthreshold characteristics of Re-S/D SOI MOSFETs with undoped and uniformly doped channel for getting more physical insight [1-3]. However, the actual doping profile after the ion implantation step differs from uniform profile and resembles much with the Gaussian profile [4]. In addition, the Gaussian profile in turn gives two more parameters, projected range (R_p) and straggle (σ_p), which can control the device characteristics.

Device structure

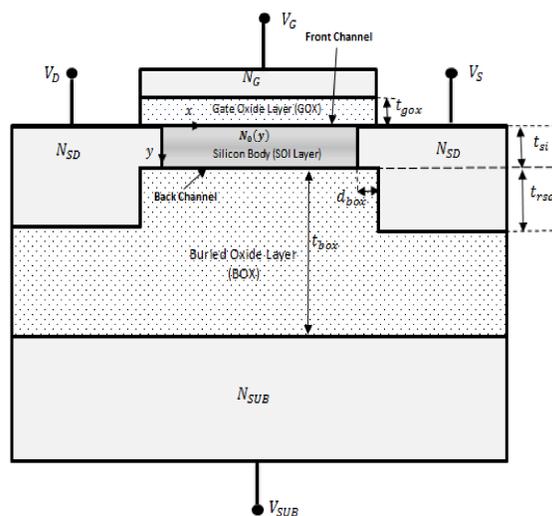


Fig. 1: Re-S/D SOI MOSFET structure showing device dimensions

The structure and schematic view of a Re-S/D SOI MOSFET, which is being considered for our model and simulation is shown in Fig.1 with channel length L , width W , channel thickness t_{si} , effective-oxide thickness t_{ox} , buried oxide (BOX) thickness t_{box} , recessed source/drain thickness t_{rsd} , and of the device respectively.

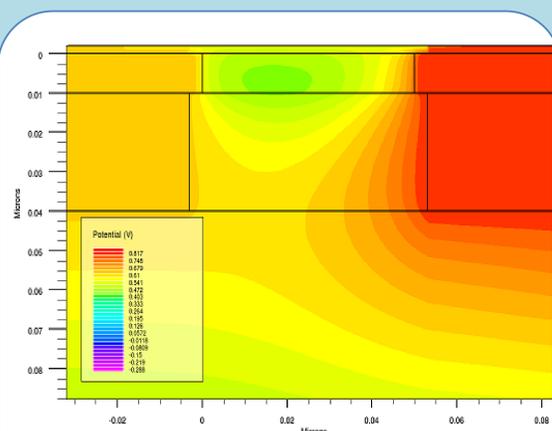


Fig. 2 The distribution of potential in the device with $L=50$ nm

Analytical Modeling

The two-dimensional (2-D) potential equation in the channel region of the recessed source/drain SOI MOSFETs which is defined by Poisson's equation, is given by

$$\frac{\partial^2 \psi(x, y)}{\partial x^2} + \frac{\partial^2 \psi(x, y)}{\partial y^2} = \frac{qN_0(y)}{k_{Si}}$$

where, $N_0(y)$ is channel concentration which is Gaussian in nature, can be expressed as:

$$N_0(y) = N_p \exp \left[-\frac{1}{2} \left(\frac{y - R_p}{\sigma_p} \right)^2 \right]$$

Electric flux at the front channel ($y=0$):

$$k_{Si} \frac{d\psi(x, y)}{dx} \Big|_{y=0} = k_{GOX} \frac{\psi - (V_G - V_{FB1})}{t_{GOX}}$$

Electric flux at the back channel ($y=t_{si}$):

$$k_{Si} \frac{d\psi(x, y)}{dx} \Big|_{y=t_{si}} = k_{BOX} \frac{(V_D - V_{FB2}) - \psi_b}{t_{RS D}} + k_{BOX} \frac{(V_S - V_{FB2}) - \psi_b}{t_{RS D}} + k_{BOX} \frac{(V_{SUB} - V_{FB2}) - \psi_b}{t_{RS D}}$$

Electric flux at the back channel ($y=t_{si}$):

$$\psi_{f,b} = A_{f,b} e^{\sqrt{\alpha_f} b x} + B_{f,b} e^{-\sqrt{\alpha_f} b x} - \frac{\beta_{f,b}}{\alpha_{f,b}}$$

where,

$$A_{f,b} = \frac{\beta_{f,b} (e^{\sqrt{\alpha_f} b L} - 1) + \alpha_{f,b} \{ V_{bi} (e^{\sqrt{\alpha_f} b L} - 1) + V_{DS} e^{\sqrt{\alpha_f} b L} \}}{\alpha_{f,b} (e^{2\sqrt{\alpha_f} b L} - 1)}$$

$$B_{f,b} = \frac{e^{\sqrt{\alpha_f} b L} [\beta_{f,b} (e^{\sqrt{\alpha_f} b L} - 1) + \alpha_{f,b} \{ V_{bi} (e^{\sqrt{\alpha_f} b L} - 1) - V_{DS} \}]}{\alpha_{f,b} (e^{2\sqrt{\alpha_f} b L} - 1)}$$

Finally, the threshold voltage can be calculated by its definition as it is the value of the gate voltage for which the minimum surface potential equals the value of two times of Fermi potential.

$$V_{th} = V_G |_{\max\{\phi_{f,min}, \phi_{b,min}\} = 2\phi_f}$$

where,

$$\phi_f = \frac{kT}{q} \ln \left(\frac{N_0}{n_i} \right)$$

The obtained threshold voltage can be expressed as

$$V_{thf} = \frac{-b_f \pm \sqrt{b_f^2 - 4a_f c_f}}{2a_f} + V_{FB1} \quad V_{thb} = \frac{-b_b \pm \sqrt{b_b^2 - 4a_b c_b}}{2a_b} + V_{FB3}$$

where, a_f, b_f, c_f, a_b, b_b and c_b are the device dependent parameters, V_{FB3} is the flat band voltage

Hence, final threshold voltage can be determined by

$$V_{th} = \begin{cases} V_{thf} & ; \psi_{f,min} > \psi_{b,min} \\ V_{thb} & ; \psi_{f,min} < \psi_{b,min} \end{cases}$$

Results and Discussion

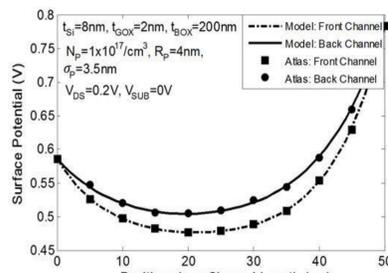


Fig. 3 The potential distribution in the channel with $L=50$ nm

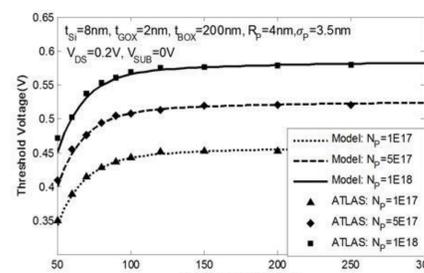


Fig. 4 Variation of the threshold voltage with gate length with Gaussian profile for different peak concentration

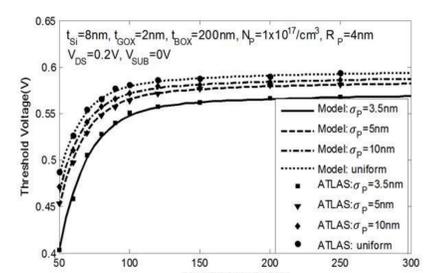


Fig. 5 Variation of the threshold voltage with gate length with Gaussian profile for different project range

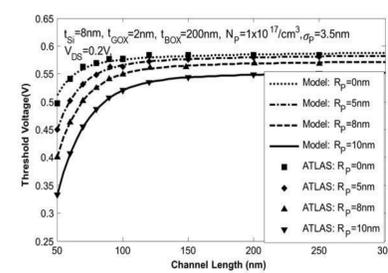


Fig. 6 Variation of the threshold voltage with gate length with Gaussian profile for different depth of recessed region

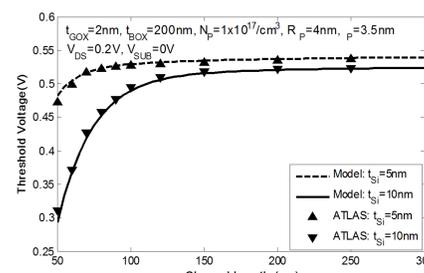


Fig. 7 Variation of the threshold voltage with gate length with Gaussian profile for different channel thickness

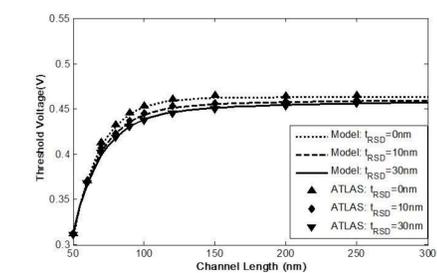


Fig. 8 Variation of the threshold voltage with gate length with Gaussian profile for different project deviation

TABLE I : Values of key parameters

Parameters	Symbol	Values	Parameters	Symbol	Values
Gate length	L_G	22nm-45nm	Source/Drain doping	N_{SD}	$1 \times 10^{20} / \text{cm}^3$
Silicon layer (SOI) thickness	t_{si}	2nm-20nm	Channel doping	N_A	$1 \times 10^{16} / \text{cm}^3$
Oxide thickness	t_{ox}	1nm-4nm	Substrate doping	N_{SUB}	$1 \times 10^{16} / \text{cm}^3$
Thickness of the source/drain extensions into the BOX	t_{rsd}	30nm	Gate voltage	V_{GS}	0.2-0.4V
Buried oxide thickness	t_{box}	100nm	Drain Voltage	V_{DS}	0.2-0.4V

Conclusion

The threshold voltage for the FD Re-SOI MOSFETs has been successfully modelled. The potential distribution is obtained using 2D Poisson's equations and proper boundary conditions by taking vertical Gaussian doping in the channel which is used to find the expression of threshold voltage. Then, this analytic model is compared by results simulated in the 2D simulator ATLAS SILVACO with different channel length (t_{si}), gate oxide (t_{GOX}), buried oxide (t_{BOX}) and recessed source/drain thickness (t_{rsd}). The model result has been matched with simulation result.

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