A Novel On-Chip Self-Testing Signature Register for Low Cost Manufacturing Test

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***Abstract*- Functional complexity, circuit density and performance of integrated circuits (ICs) are persistently escalating. Test data generated for such ICs, using *de facto* scan test, is expanding beyond gigabits. Precise comparison of such bulky data on automatic test equipment (ATE) demands huge memory, large number of scan channels, multiple drive and compare edges per tester cycle and augmented test time, that are collectively increasing test cost. In this paper an on-chip self-testing signature register is proposed which compact the test response and compares generated test signature with golden one, generating two bits of PASS/FAIL test result on single pin. This significantly reduces memory and scan channel requirement on ATE. Furthermore for 50% increase in scan chains, 32.70% reduction in test time is observed with little area overhead of 4.25% on scan design. The proposed architecture has also been validated through FPGA implementation.**

***Keywords:* ATE memory, design for testability (DFT), signature register, test cost, test time, tester channel reduction.**

I. INTRODUCTION

Design for Testability (DFT) has become an integral part of modern ASIC design flow. Improved DFT structures along with efficient Automatic Test Pattern Generation (ATPG) algorithms assist high quality tests of complex ASICs. Post-silicon validation of design includes evaluation and characterization of ICs. It identifies logical and electrical bugs in design before sending the same for mass production. These tests are time taking and involve rigorous analysis. In contrast, manufacturing tests make PASS/FAIL decision by targeting fabrication defects in a large volume of ICs. These must be completed within a short interval of time. But, downloading responses from design under test (DUT) and the number of compare edges required on an ATE make test time exorbitantly large.

The cost of manufacturing test is governed by the resource utilization of ATE. For this, test engineers have to consider ATE resources, such as memory depth, number of pins, and number of drive and compare edges per tester cycle, before selecting an ATE for testing. Moreover, recurring test cost of a chip directly depends upon test time that includes time required to load test program, apply test vectors and analyze response of the chip. In standard scan-based test, test responses go back to the ATE for comparison with golden responses [1]. But, downloading such bulky data from the DUT to the ATE memory and comparing the same with the desired one add up considerable time [2]. Furthermore, increasing number of flip flops in scan based design increases test time linearly [1]. To avoid this, DFT engineers are forced to use more number of scan chains. However, increasing number of scan chains is limited by available tester channels for scan operation and also generates more test response data in turn demanding additional tester memory. Besides, 20% of modern chips fail due to presence of delay defect alone [3]. Performing precise delay test demands higher buffer capacity and ATE timing accuracy [4]. These factors collectively push the test cost up; challenging DFT engineers to implement scan design effectively. The work presented in this paper is mainly focused on output compaction. The two classes of output response compactors, seen in literatures, are based on time compaction and space compaction. Space compactor compacts width of patterns. But, it has very less compaction ratio. Time compactor compacts number of patterns. This includes counting based techniques, parity check and signature analysis [6]-[11]. A reliable scan based output compactor must have very high compaction ratios and design simplicity. Developed at Hewlett-Pickard, the signature analyzer has proved to be extremely efficient tool for catching faults in bit stream and diagnostic purpose [12].

Mostly, signature analyzers use Linear Feedback Shift Register (LFSR) as response compactors [12]. This can be used in two configurations. The first configuration uses a remainder in the LFSR as test signature [2]. At the end of the test, this signature is downloaded on ATE and compared with a golden one. This is capable of compacting gigabits of test response to a small signature, depending on length of the signature register (say16, 32 or 64 bit long). But here, there is no reduction in number of tester channels. The second configuration uses a bit stream that is sent out of the signature register at every clock pulse as a signature [12]. For N scan chains fed to signature register, this configuration gives significant reduction in test pin count by the factor of N. But, this in turn demands sufficient tester memory and large number of compare edges on ATE.

To address these issues, we introduce self-testing signature register for test response compaction and comparison. In this, the remainder in signature register is used as signature and the embedded comparator facilitates test signature comparison with golden signature to generate a single bit test status signal, irrespective of number of scan chains. Being no test response storage is demanded on ATE memory, this considerably reduces the usually requirement of large tester memory. Also, with only single pin to be monitored for test result, the number of tester channels and compare edges on ATE side significantly reduce at the end of the test. This cut down maintenance and usage cost of test floor and increases its life time. This also gives scope for DFT engineers to increase number of scan chains so as to reduce test time.

Rest of the paper is organized as follows. In section II, preliminaries are discussed. Section III and IV, explain the main idea and its implementation. Section V shows experimental results. Finally, section VI concludes this paper.

II. PRELIMINARIES

A. Previous Work :

LFSR based signature register is a popular and efficient output response analysis tool [12]. Most of the industrial designs use on-chip LFSRs to generate small signatures during manufacturing test. In last three decades, researchers identified several issues with LFSR based signature analysis schemes that are: improving signature register design to minimize the cost of testing, handling X-states propagating into signature registers, selection of the 'best' polynomial defining the feedback, minimization of probability of

fault masking and besides testing, its support for debugging and diagnosis of a chip [11] [13]-[16]. In this work, the focus is mainly on techniques for reduction in test time and cost during manufacturing test.

To address the problem of test cost and test time, a number of output response compaction schemes have been proposed [2] [17]-[19]. Barnhart et.al proposed a technique called on-product MISR (OPMISR) [2]. This utilizes IBM's logic BIST structure called STUMPS [20] in which MISR structure is used at the output of product scan chains. In comparison with conventional scan methodology, the OPMISR technique compact the test response and reduces the number of test cycles required for testing a chip on ATE. But at the same time, it demands a large amount of ATE memory buffer. Also, no reduction has been observed in tester channel requirement. An improved MISR design is proposed in [21]. In this, instead of feeding the scan-out data directly to multiple input signature register, first it is aggregated and then is fed into single input shift register. This makes operation of the MISR tractable and guarantees irreducibility for all input divisor polynomials.

Another significant contribution to address test time is EDT. EDT technique incorporate both input decompression and output compression. Output compaction is built on XOR trees [26].

On-chip comparison based schemes are found in literature to address the problem of test cost and test time. This technique is attractive solution, because of its complexity in design. The probability of false negatives and false positive is comparatively less [24]. The pass/fail signature is generated based on the comparison between the expected responses and response obtained from device under test. On-chip comparison is performed using XOR gates [24].

On-chip comparison technique proposed in [24] makes use of on-chip memory unit to store the expected responses. The output compaction circuit developed is mainly focused to help diagnosis, not production testing.

The load board or DUT board used in production testing on ATE's can carry comparison circuit to generate pass/fail signature [27].

The on-chip comparison technique is also found in testing of cryptographic circuits. The main objective of using on-chip comparison technique is to prevent sensitive data coming out of chip during testing. Security analysis shows it is suitable for cryptographic testing [25] [28].

Our research is to improve the on-chip comparison technique for betterment of test time and test cost. On-chip comparison circuit in [24] makes use of memory unit and loading the expected responses into memory on ATE is more time consuming. [24] Work is focused on diagnosis.

Designing comparison circuit on DUT boards as in [27] is not a recommended practice. DUT boards are electro-statically sensitive and having large circuits on DUT board will further create problems in production environment like during interface with handlers etc. And this technique also escalates the design and manufacturing cost of DUT board.

The on-chip comparison techniques mentioned above focused on diagnosis and cryptographic circuit testing. The usage of on-chip comparison scheme for test time and test cost reduction is not addressed in above mentioned literature. The past research also lacks analysis with respect to ATE resources such as pattern memory, number of scan channels, number of compare edges and test time for on-chip comparison technique.

The possible techniques to reduce the cost of production testing are to utilize less ATE resources such as memory, scan channels, drive and compare edges per tester cycle and to minimize test time per chip. In this paper, we propose self-testing signature register design targets to reduce the tester time and the number of ATE test channels.

III. Main Idea

The proposed self-testing signature register is basically an on-chip test output response compaction and signature comparison architecture generating a single bit PASS/FAIL test result to be monitored. Fig. 1 (a) shows schematic of proposed architecture. Output response compaction block, SR, uses either of *N*-bit signature register shown in Fig. 1 to generate 'sufficiently' unique signature for a given bit stream. SISR is a dedicated signature register per scan chain whereas MISR, depending on its length, can generate a signature conjointly for scan chains. Also, the golden signature for particular set of test patterns is calculated with knowledge of scan-out bit stream generated by simulator and can be loaded into latch chain LC, concurrently with application of test patterns. The gate level schematic of latch chain is shown in Fig. 2 (b). At the end of test, an Ex-OR operation is performed between test and golden signatures. Further, Bitwise OR operation is conducted on the result of Ex-OR operation, to identify any mismatch in signatures. This generates final PASS/FAIL test result for that particular test.

As shown in Fig. 1 (a), SO_i are input to SR that is connected to scan-out signals in design and *LSI* is latch chain input used for loading reference signature in latch chain. *s_clk* and *latch_clk* are clock signals for driving signature register and latch chain. The clock used for driving signature register is same as scan clock for DUT. However, any clock signal can be used for loading latch chain. To control the clocking of signature register and latch, separate signature enable *SEn*, and latch enable *LEn*, signals are provided. *latch_clk* is disabled after loading last bit (MSB) of golden signature into latch chain, while *s_clk* is disabled once all test patterns are applied to DUT. This avoids unnecessary transition of signature register after

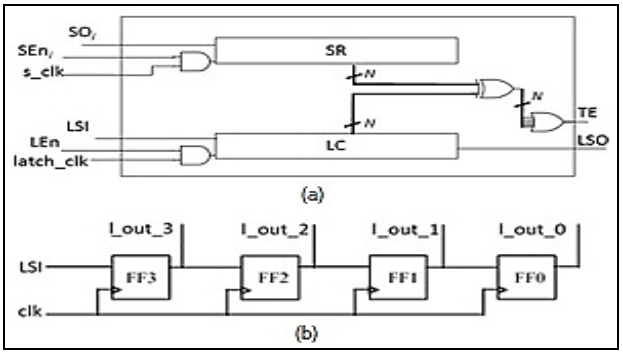

Fig. 1. Schematic of (a) proposed self-testing signature-register and (b) Latch chain

completion of scan-out operation and stabilizes the signature for comparison. In case of multiple self-testing signature-registers in design, latch chains could be further chained by connecting latch output, *LSO*, to *LSI* of next latch chain. By doing this, single *LSI* pin can be used to load all latch chains. Also, OR operation of all *TE* pins can be performed to obtain test result of entire chip.

IV. IMPLEMENTATION

A. Scan Design:

Fig. 2 shows gate level description of conventional scan flip flop used as DFT. The lines *D*, *Q*, and *clk* are the input, output and clock lines respectively. The lines *SI* and *SO* are the input and output for constructing scan path. The output *SO* is connected to *SI* of an adjacent scan flip-flop or a primary output *SCANOUT*. The input *SI* is connected to *SO* of an adjacent scan flip-flop or a primary input *SCANIN*. The line *TM* controls multiplexer for defining mode of operation. When *TM* = 0, the flip-flop is in normal mode of operation. When *TM* = 1, the flip-flop is in scan mode of operation.

B. Design Of Signature Register:

Targeted probability of fault masking, selection of feedback taps and P-P-A matrix has to be considered during design procedure of signature register. In experimentation with proposed design, 16 bit signature register is chosen. Using eq. (1), it has theoretical aliasing probability value of

$$\frac{1}{2^{16}} = 0.000015$$

This gives fault detection probability of 99.9985% per 16 bits of input bit stream. Note that this is the pessimistic theoretical value. Chosen a proper characteristic polynomial defining feedback, it has proven s excellent in fault detecting capability in scan-out bit stream. Besides, on performance point of view, it has been seen that, for a given characteristic polynomial, internal feedback configuration of LFSR has higher operating frequency than its external feedback counterpart. Thus, keeping in mind an at-speed testing of today's high performance VLSI ICs, internal feedback configuration is chosen for signature register design. Furthermore, the polynomial defining the feedback divides the input bit stream and the remainder stays back in the LFSR stages as signature. For the 'sufficient' uniqueness of signature, the chosen polynomial must provide a large pool of different reminders. Thus, the largest possible primitive polynomial is selected for the given length of LFSR. This will allow LFSR to cycle through maximum length pseudo-random sequence rather than some shorter trivial sequence.

C. Design Of Self-Testing Signature Register:

The use of signature analyzer alone does not change the demand of the ATE channels. Thus, a novel self-testing mechanism is incorporated in LFSR. In existing designs, the remainder present in the signature register will be latched into ATE for comparison. This

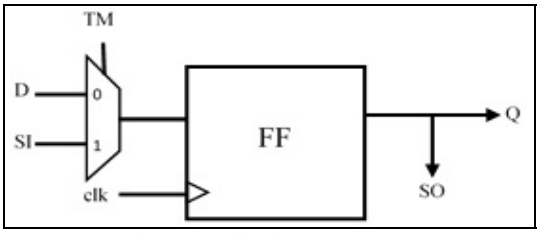

Fig. 2. Scan flip flop used as DFT

requires ATE channels equal to bit-length of signature register. The proposed design facilitates to store golden signature and compare same with test signature reducing the demand of ATE channels significantly. Realizing this self-testing signature register carries signature register as a response compactor, a latch chain to store golden signature and a cascade of Ex-OR and OR gates as comparator. Latch chain is a serial-in parallel-out (SIPO) architecture of *N*-bit shift register. With the proposed design, single ATE channel is sufficient to analyze the test result.

Fig. 1 (a) shows architecture of the proposed self-testing signature register. It uses *LSI* pin to serially shift golden signature into latch chain. Both input patterns and golden response can be fed concurrently to DUT (*SEn = LEn = 1*) and once data is stored into latch, *LEn* signal is disabled (*LEn = 0*). This this does not intervene in application of test patterns at input side. For *p* scan chains, this architecture demands *(p+4)* ATE channels (p channels for scan-in and one each for latch enable, signature enable, latch input and test result). Also, in case of variable-clock scan test [23], a slow clock may be applied for latching in golden signature. This gives enough confidence for correctness of data stored in latch chain by giving sufficient time for logic to settle at the input of each memory element in scan chain. In case of SISR based system, primary input scan-in can also be used to latch data in latch chain, further reducing a test pin. This is shown in Fig. 3.

D. Whole System:

Fig. 4 shows the entire proposed system. This consists of a 'low cost' tester and a chip designed with embedded self-testing signature register (STSR). The 'low cost' tester refers to a tester with minimum utilization of its resources such as memory, scan channels and that adds to less tariff. It is assumed that all flip flops on a chip are grouped to form *p*-scan chain. Each scan chain has its own scan-in line SI_i. Test mode, reset, and clock lines of all flip-flops are combined to single lines *TM*, *rst*, *clk* lines respectively. Scan chains are further grouped in *m* groups such that all scan-out signals in one group are fed to one self-testing MISR ($STSR_i$). Thus, as a whole, *m* STSR blocks are required in design. Latch clock and enable signal for signature register and latch are again combined to single lines *latch_clk*, *SEn* and *LEn* respectively. All latch chains are further chained with *LSI* as single latch input. *TR* is the test result of entire chip given back to ATE for test decision.

In designs with small flip-flop count and no clock domain crossing, a single scan chain can be used for testing. Such designs can utilize self-testing SISR.

E. Test of Proposed Architecture:

The signature analyzer has to be verified for its capability to detect manufacturing defects in DUT. Due to randomness in generated signature, functional test is enough to validate operation of the signature register. Thus, this can be easily tested without generating any special patterns or addition of any DFT structures. A toggle sequence, for example, 00110011…, used for testing the scan register can be allowed to enter into STSR to generate signature for the same.

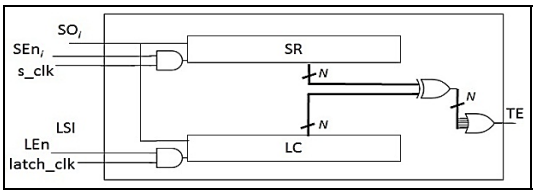

Fig. 3. Schematic of self-testing SISR using scan chain to load latch chain

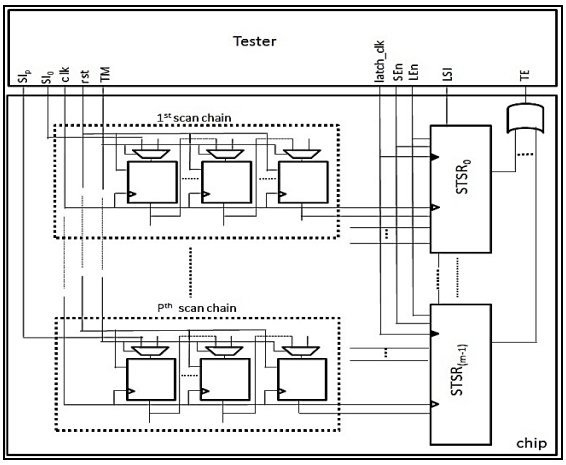

Fig. 4. Whole system

Generated signature is compared with desired one to validate the operation of STSR, as stated earlier.

V. Experimental Results

In this section, we present the experimental results. The proposed embedded test architecture is compared with conventional scan methods for various parameters. An experiment has been performed in two phases. First phase is simulation based that includes test pattern generation, test response collection, golden signature calculation and simulation based validation of test result generated by proposed architecture in presence of injected faults. While second phase includes FPGA implementation of design with proposed architecture, application of generated test patterns to it and its validation again in presence of injected faults.

Relatively larger ISCAS'89 sequential benchmark circuits are selected for experimentation. The scan clock frequency and operating frequency of design are considered to be same in order to validate the proposed design for at-speed testing. The length of LFSR used is 16 bit. The biggest possible primitive polynomial is used for defining feedback taps along the LFSR. Each design under consideration is tightly constrained for timing with sufficient on-path slack and minimum area and power. In the first phase of experiment, the designs are synthesized with TSMC 65 nm technology library using Synopsys design compiler. TSMC8K_Lowk_Conservative wireload model has been considered for interconnects and multiplexed flip-flop as DFT. Also, scan pins in test mode are multiplexed with pins in normal mode with addition of extra test mode pin to switch mode of operation of DUT. In this experiment, multiple scan chains are used for first five large benchmark circuits, while single scan chain is used for others. To deduce information about delay paths and to check timing violations of design, static timing analysis (STA) has been performed using PrimeTime, Test patterns for testing stuck-at faults and path delay faults are generated using TetraMAX, an ATPG tool by Synopsys.

Then, in second phase of the experiment, DFT structure inserted benchmark circuits with addition of proposed architecture are synthesized in Xilinx environment and downloaded in Virtex 2 Pro FPGA (Board 1).Also, FSM for applying TetraMAX generated test is downloaded in another FPGA (Board 2). This board 2 can be assumed to be a realization of ATE on FPGA for application of test patterns to board 1. The final single bit test result is validated in fault-free designs and in designs with injected faults.

For comparison with conventional designs, overhead of proposed design in terms of area and FPGA slice count are defined as follows:

$$O_A = (A_{PROP} / A_{SCAN} - 1) \times 100\ \% \quad (2)$$
$$O'_A = (A_{PROP} / A_{CONV} - 1) \times 100\ \% \quad (3)$$
$$O_S = (S_{PROP} / S_{SCAN} - 1) \times 100\ \% \quad (4)$$
$$O'_S = (S_{PROP} / S_{CONV} - 1) \times 100\ \% \quad (5)$$

Here, O, A, and S denote Overhead, Area and Slice count respectively while suffixes *PROP, SCAN, and CONV* denote circuits implemented with proposed test architecture, that with only scan chain inserted and that which uses conventional signature register for response compaction [2], respectively. Also, the primed character signifies overhead of proposed architecture on standard scan design and the unprimed ones signify overhead on conventional signature register. Further, the reduction ratio of test pins (R_C), and that of test time is defined as:

$$R_C = (1 - C_{PROP} / C_{CONV}) \times 100\ \% \quad (6)$$
$$R_T = (1 - T_{PROP} / T_{CONV}) \times 100\ \% \quad (7)$$

Here, C is total number of tester channels, T is test time and suffixes have the same meanings as discussed above.

A. Memory Requirement:

This refers to ATE memory required for response collection from chip during the progress of test. Table I shows number of patterns generated and fault-free output data volume collected after simulation of listed benchmark circuits. The columns N_{SAF} and N_{PDF} are the number of test patterns generated targeting stuck-at faults (SAF) and path delay faults (PDF) in design respectively. The columns V_{SAF} and V_{PDF} are number of output response bits collected, whereas, the column V_{SCAN} is the total response collected in SAF and PDF test. It can be seen from Table I that, using conventional scan test methodology, on an average 8100 test responses have to be downloaded from chip and same number of golden responses has to be pre-stored on ATE memory for comparison, in stuck-at fault test alone. This number turns out to be 15850 for designs with multiple scan chains (an average of V_{SCAN} for first five benchmark circuits in Table I). Similarly, average response count for path delay test is around 4000. In line of these results, test of today's VLSI designs demand enormously high ATE memory requirement. This puts an extra constraint on ATPG tool to generate less number of test patterns. Also, in a conventional signature register, the number of signature bits to be downloaded on ATE will be equal to double the bit length of signature register. In contrast, the proposed architecture requires only two bits for comparison on ATE irrespective of bit-length of MISR and number of scan chains in design. This significantly reduces requirement of ATE memory buffer.

B. Test Time Reduction:

Table II compares test time reduction using proposed architecture. The column N_{FF} is number of flip flops in design. Also, Time reduction ratio in last column is calculated using eq. (7). As less number of tester channels are demanded using proposed architecture, the number of scan chains can further be increased to reduce test time of a chip. In this experiment, 50% more number of scan chains are inserted using proposed architecture, compared to conventional one. On an average, 33% reduction in test time is observed. This is due to generation of less number of patterns generated with increased number of scan chains.

TABLE I
DATA VOLUME

Benchmark Circuits	N_{SAF}	N_{PDF}	V_{SAF}	V_{PDF}	V_{SCAN}	V_{CONV}	V_{PROP}
S35932	49	15	1656	662	2318	32	2
S38584	806	356	25082	17765	42847	24	2
S38417	1054	270	35177	13598	48775	32	2
S15850	458	135	10110	4182	14292	32	2
S13207	409	125	7284	3618	10902	20	2
S9234	178	15	393	44	437	32	2
S5378	274	35	476	92	568	32	2
S1488	145	24	275	52	327	32	2
S1423	101	10	225	26	251	32	2
S1238	212	11	335	20	355	32	2
Average	-	-	8101.3	4005.9	12107.2	30	2

TABLE II
TEST TIME ANALYSIS

Benchmark Circuits	Using Conventional signature register			Using Proposed Architecture			Reduction Ratio	
	N_{SC}	T_{SAF} (ns)	T_{PDF} (ns)	N_{SC}	T_{SAF} (ns)	T_{PDF} (ns)	RT_{SAF} (%)	RT_{PDF} (%)
S35932	16	24800	7100	24	15400	4600	37.90	35.21
S38584	12	388800	143500	28	260200	97300	33.08	32.19
S38417	16	522300	109500	24	357600	75600	31.53	30.95
S15850	10	228900	56300	15	141900	36400	38.00	35.35
S13207	10	188600	52900	15	135800	36300	28.00	31.38
Average	-	270680	73860	-	182180	50040	32.70	32.25

C.ATE Test Channels Reduction:

Design with self-testing MISR shows significant reduction in demand of tester channels compared with conventional scan test with multiple scan chains. Table III shows tester scan channel requirement for both conventional and proposed test methodology. The value in last column is calculated using eq. (6). It can be seen that, for P scan chains in a design, conventional scan methodology and conventional signature register demands minimum $(2P + 2)$ ATE scan channels, whereas, this number is $(P + 4)$ for proposed architecture. Thus the reduction ratio turns out to be

$$R_C = \frac{P-2}{2(P+1)} \times 100\ \% \qquad (8)$$

As the number of scan channels increases, which is necessary to reduce test application time, R_C approaches a value of 50 %. Same analysis is shown graphically in Fig. 6 Reduction in tester channels gives a broader scope for increasing scan chains during the process of DFT insertion.

D.Area Overhead:

Table IV shows the area comparison between conventional and proposed signature register for both ASIC and FPGA implementation. The FPGA used is Xilinx Virtex II Pro. The column N_{FF} is number of

TABLE III
ATE SCAN CHANNEL COUNT

# Scan Chains	# Scan Channels		R_C (%)
	CONV	PROP	
10	22	13	40.90
12	26	15	42.30
16	34	19	44.11

TABLE IV
AREA AND FPGA UTILIZATION ANALYSIS

Benchmark Circuits	N_{FF}	N_{SC}	Area for 65 nm TSMC library					Slice count for Xilinx Virtex II Pro FPGA				
			A_{SCAN}	A_{CONV}	A_{PROP}	O_A (%)	O'_A (%)	S_{SCAN}	S_{CONV}	S_{PROP}	O_S (%)	O'_S (%)
S35932	1728	16	24526.80	24707.16	24979.21	1.84	1.10	3028	3037	3061	1.09	0.79
S38584	1426	12	21245.40	21425.76	21641.50	1.86	1.00	3222	3231	3257	1.09	0.80
S38417	1636	16	22700.52	22880.88	23152.92	1.99	1.19	3109	3118	3161	1.67	1.38
S15850	534	10	7808.76	7989.12	8176.40	4.70	2.34	1088	1097	1125	3.40	2.55
S13207	638	10	8108.64	8289.00	8476.29	4.53	2.26	1070	1080	1098	2.61	1.67
S9234	211	1	2209.68	2210.68	2584.44	16.95	16.90	328	338	353	7.62	4.44
S5378	179	1	2805.48	2806.48	3180.24	13.35	13.31	404	414	429	6.18	3.62
S1488	6	1	697.32	698.32	1072.08	53.74	53.52	141	150	169	19.85	12.67
S1423	74	1	1249.92	1250.92	1624.68	29.98	29.88	240	250	266	10.83	6.40
S1238	18	1	714.96	715.96	1089.72	52.41	52.20	134	143	163	21.64	13.98
Average	-	-	9206.75	9297.43	9597.75	4.25	3.25	1276	1285	1308	2.50	1.79

flip flops in design. It can be seen that, proposed embedded test architecture shows very small overhead compared to both ASIC and FPGA implementation. On an average, proposed architecture occupies 3.25% more area than conventional signature register. And also, FPGA utilization in increased by 2.5%. Fig. 6 and 7 shows the tabulated data in Table IV in graphical form.

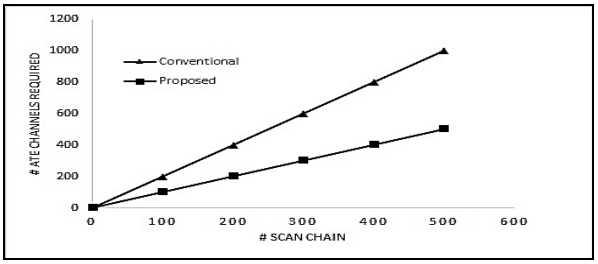

Fig. 5. Comparison for ATE channels requirement v/s scan chain count

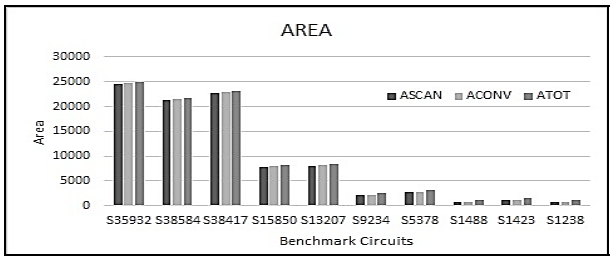

Fig. 6. Area overhead comparison for benchmark circuits

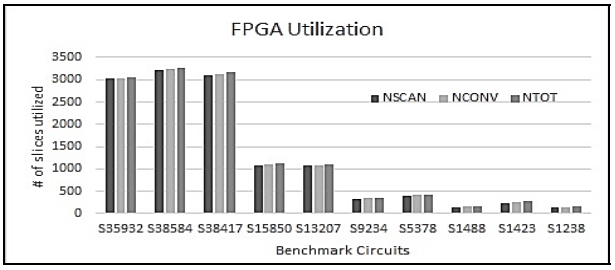

Fig. 7. FPGA utilization overhead comparison for benchmark circuits

VI. CONCLUSIONS

A novel self-testing signature register has been proposed for scan based manufacturing test. At the end of the test, this generates PASS/FAIL test result on single pin, and only two bits are required for comparison on ATE. This minimizes requirement of huge ATE memory and multiple compare edges per tester cycle. Also, proposed architecture considerably reduces test pins on chip and hence tester channels, allowing DFT engineers to incorporate more number of scan chains during design phase to reduce test time. Reduced test time and usage of minimum ATE resource such as memory, scan channels and compare edges per tester cycle cut down ATE tariff for manufacturing test.

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