Design of Low-Leakage and High Stable Proposed SRAM cell Structure

Debasish Nayak¹ Dept. Electronics and Communication Engineering National Institute of Technology Rourkela, India ¹nayak.debasish84@gmail.com D.P.Acharya² Dept. Electronics and Communication Engineering National Institute of Technology Rourkela, India ²d_p_acharya@rediffmail.com

Abstract— The high demand of embedding more and more functionality in a single chip has enforced the use of scaling. As scaling drastically reduce the channel length the leakage current also increases significantly which increases the static power dissipation. A novel 8T-SRAM cell (Leakage Current Reduced SRAM cell) is proposed which reduces the leakage power dissipation significantly in comparison to the conventional 6T-SRAM cell. The cell is designed using GPDK-90 nm technology library and simulated under Cadence Virtuoso design environment. The proposed cell uses a lower voltage than V_{dd} during standby mode which leads to a reduction of leakage current and hence the static power consumption. The lower voltage is generated using an NMOS which creates a threshold voltage drop when transfer a high logic. The power consumption is found to be 25.02 % lesser than that of conventional six transistors SRAM cell .The stability and the write ability are measured using the N-Curve technique.

Index Terms— Leakage current, Leakage power, Static power, Low power, stability, N-Curve, SVNM, SINM, WTV, WTI

I. INTRODUCTION

As there is a high demand to use multiple functionalities in a single portable gadget, the prime objective of the IC designer has become to reduce the size and power consumption of the chip. Among the several methods which are employed to reduce the silicon area and the power consumption; device scaling is the widely used one. Two most important parameters on which design engineer mostly relay are the sizing of transistor and operating voltage.

Dynamic power consumption can be reduced by reducing the supply voltage. But reduction in supply voltage leads to a reduction in performance. To avoid this performance degradation the threshold voltage of the cell should also be scaled down. But the sub-threshold leakage current increases exponentially with the decrease in the threshold voltage. This leads to an exponential increase in the static power consumption. This is because static power dissipation is mainly contributed by sub-threshold leakage current and gate leakage current [1]. Hence in the deep sub-micron technology the static power has also become a major concern along with the dynamic power.

Recent studies show that the memory block is occupies a major portion of the SoC. A large number of memory cells combine to form a memory block. Hence a large amount of performance enhancement can be achieved by improving a small amount of performance in a single memory cell. Hence Prakash Kumar Rout³ Dept. Electronics and Communication Engineering Silicon Institute of Technology Bhubaneswar, India ³Prakashrout05@gmail.com K.K.Mahapatra⁴ Dept. Electronics and Communication Engineering National Institute of Technology Rourkela, India ⁴kkm@nitrkl.ac.in

memory cell can be good target to achieve performance. To reduce the leakage power dissipation of the memory block, researchers have employed several techniques such as supply voltage gating during sleep mode [2], virtual ground during standby mode [3], and switching off the unused portion of cache [4] etc. The technique employed in [3], needs an additional voltage source for the virtual ground concept. The techniques employed in [2, 4] use additional circuits and power to identify the unused portion of the memory block. Here we propose a novel leakage current reduced SRAM (LCR-SRAM) which don't use any additional voltage source. The property of the NMOS, "not to conduct high logic properly" is used to generate a lower voltage than V_{dd}, which is used as supply when the cell goes to standby mode. The reduction in the operating voltage during standby mode reduces its leakage current flow and hence its static power consumption.

The rest part of this paper is organized as follows. The proposed LCR-SRAM cell is presented in section II. The result and analysis is presented in section III, the stability analysis is presented in section IV. Finally section V represents the conclusion.

II. THE PROPOSED LCR SRAM CELL

Figure 1 represents the transistor level diagram of the leakage current reduced SRAM (LCR-SRAM). NM1-NM4 and PM1-PM2 basically forms a conventional 6T SRAM cell. This is combined with two additional transistors NM5 and PM3. The cross coupled inverters is connected to V_{dd} through NM5 and PM3. As the gate of NM5 is connected to V_{dd} it always remains on. The transistor PM3 lies parallel to NM5. The gate of PM3 is supplied a signal WLB to switch it on during active mode and to switch it off during standby mode.

The sub-threshold leakage equation described in BSIM2 model as given in equation 1 and 2 [5]

$$I_{leakage} = I_0 \exp \frac{\frac{-Vto-\gamma \cdot V_{bs} + \eta V_{ds}}{\eta V_{th}}}{\left(1 - e^{\frac{-V_{ds}}{V_T}}\right)}$$
(1)

Where
$$I_0 = \mu_0 c_{0x} V_{th}^2 e^{1.8} \left(\frac{W_{eff}}{L_{eff}} \right)$$
 (2)

The μ_0 stands for mobility, C_{ox} is the oxide capacitance, W_{eff} and L_{eff} are effective width and length respectively, γ stands for the body effect coefficient, V_{bs} is the body-source voltage, V_{t0} stands for threshold voltage, η is the DIBL coefficient and V_{ds} is the drain source voltage.

Clearly it can be found from the equation 1 that the reduction in V_{ds} decreases the leakage current. This trick is used in the proposed LCR-SRAM cell to reduce the sub-threshold current. The property of the NMOS, not to conduct high logic poorly is used to generate a lower voltage level V'_{dd} at the source of NM5. This reduced voltage source V'_{dd} is supplied to the cross coupled inverter during standby mode which significantly reduce the sub-threshold current. As static power is majorly contributed by the sub-threshold leakage current hence the reduction in leakage current leads to a reduction in the static power as well as.

When the WLB signal goes high PM3 turns off and NM5 is the only path between $V_{dd} \& V'_{dd}$ node. As NMOS restricts the transfer of high logic up to V_{dd} - V_{th} , the V'_{dd} node can charge maximum up to V_{dd} - V_{th} . When WLB goes low PM3 turns on. As PM3 can conduct high logic perfectly the V'_{dd} node can charge maximum up to V_{dd} . So the V'_{dd} becomes equal to V_{dd} during WLB low and the V'_{dd} become equal to V_{dd} - V_{th} during WLB high. Equation 1 indicates that the sub-threshold current of PM1 & PM2 are highly dependent on its V_{ds} value. Hence the reduction in V'_{dd} will reduce the drain to source voltage of PM1 & PM2 and as a result it reduces the sub-threshold leakage current.

The LCR-SRAM can be operated in two different modes. They are active mode and standby mode. The active mode is employed for any read or write operation of the LCR-SRAM. Because In active mode of operation initially the WLB node is lowered which turns on the PM3 allowing V'_{dd} to charge up to V_{dd} . This ensures the voltage at the internal nodes to be a proper high logic value. Then the WL node goes high which turns on the access transistor and hence the bit line can access the core of the cell.

All the time when no read or write operation is in process the LCR-SRAM is push in to the standby mode. Once the data is stored in to the cell the internal node V'_{dd} can be lowered to $(V_{dd} - V_{th})$ by activating the WLB line. As V'_{dd} reduces, the V_{ds} across the pull up transistors decreases and hence the sub-threshold current of the pull up transistor also decreases. This leads to a significant leakage reduction and hence energy reduction.

As any read or write operation of the SRAM cell can happen by switching on the access transistor, it should be ensured that the degraded node should be restored before switching on the access transistor. For restoring the degraded node the WLB signal should be kept low which switches on PM3 and allows the V'_{dd} node to charge up to V_{dd} . Hence to ensure a correct logic the WLB should be low before the WL goes high and WLB should go high after WL goes low. This can be done by choosing WL and WLB two non-overlapping signals.



Fig. 1. Schematic of proposed SRAM cell

III. PERFORMANCE ANALYSIS OF THE LCR-SRAM CELL

The LCR-SRAM is designed using GPDK 90-nm technology in cadence design environment. A spectre simulation is performed using GPDK 90-nm technology in the cadence design environment for the LCR-SRAM cell. The simulation is performed at room temperature $(27^{\circ}C)$ with a 1V power supply.

During the read operation, the bit lines are pre-charged to V_{dd} level and then the access transistors are enabled. Then the node storing 0 pulls down its corresponding bit line whereas the other node does not pull down its corresponding bit line. The sense amplifier attached to both the bit lines can sense it and can predict the data stored.

In this above process there is a chance of the 0-node to elevate itself, by the influence of the high voltage of its corresponding beat line. This elevation of the 0-node should be limited till the switching threshold voltage of the cell which ensures that the state of the cell is unchanged. This can be achieved by keeping the resistance of the access transistor larger than that of pull down transistors. The aspect ratio of the access transistor to the pull down transistor should be chosen carefully [6] so that the resistance of the access transistor will be more than the resistance of the pull down transistor. Hence the width of all the access transistors, pull up transistors, NM5 & PM3 is set to 120nm whereas the width of the pull down transistors is kept 240nm. The length of all the transistors is set to the minimum value possible in the used technology, i.e. 100nm. Figure 2 depicts the transient analysis of the LCR-SRAM.

Figure 2 reveals that when WL signal goes low the high logic stored in the internal node 'q' or 'qb' is degraded by a threshold voltage drop. This should be restored before the access transistor activate again i.e. before the WL signal goes high again. For restoration of the degraded high logic the WLB signal is made low so that PM3 will be on. Hence V'_{dd} node can be charge up to V_{dd}. To ensure the logic restoration the proposed cell uses two non-overlapping signals WL and WLB. WL and WLB signal are chosen to be non-overlapping to ensure that WLB goes low before the WL signal goes high and WLB goes high after WL signal goes low.

Figure 3 illustrates the restoration concept of the proposed LCR-SRAM design at node 'q'. A particular case in the simulation represents WLB node goes low at 194 ns and the WL node goes high at 195 ns. Till the time WLB is not lowered the 'q' node remains at 822 mV, but as soon as the WLB goes is lowered at 194 ns, the q node starts to charge up. It achieves a voltage of 990.7 mV by 194.1 ns. This ensures a perfect high logic at the 'q' node.

observed that the static power consumption (when WL = 0) from 77 ns to 120 ns is 16.693nW. At 120 ns the WL is low the BLB node goes high whereas the qb node continues to store a low logic. Hence the access transistor NM3 is off but the V_{ds} across it increases which leads to increase in its leakage current. Hence from 120 ns to 194 ns the static power consumption is 54.921 nW.



Fig. 3 Restoration of the degraded q node containing high logic

Figure 4 represents the pattern for the transient power consumption of the proposed cell. It seems almost flat and glitches in between. These glitches are due to the dynamic power consumption during the state transition. The power consumption in the rest portion of the plot is due to the static power which is mainly due to the leakage current. It seems to be 0 but actually it is in the nano-watt scale. The actual value of the static power is shown clearly in figure 5. It is clearly



Fig. 4 The transient power consumption of LCR-SRAM cell



Comparison of the static power consumption of the LCR-SRAM is made with that of a conventional SRAM. A conventional 6T-SRAM having the similar W/L ratio as the LCR-SRAM is designed and transient analysis is carried out. The operating voltage is set to be 1V and the operating temperature is set to be the room temperature, i.e. 27^oC. The same bit line and word line pulses are engaged for simulation of the conventional SRAM as that of LCR-SRAM.

Figure 6 represents the transient analysis output of the conventional SRAM. Figure 7 represents the static power consumption of it. Comparison between the figure 5 and figure 7 represents that LCR-SRAM consumes much less static power in comparison to the conventional SRAM. Because for conventional 6T-SRAM cell from 77ns to 120ns the static power consumption is 27.98nW whereas for LCR-SRAM that is 16.693nW, i.e. a 40.33% of reduction. Similarly from 120ns to 194ns the static power consumption for conventional SRAM is 78.057nW whereas in case of LCR-SRAM that is 54.92nW, i.e. a 29.64% reduction. The key factor behind the reduction in the static power is the reduction of the V'_{dd} voltage during the standby mode.





Fig. 7 Static power consumption of 6T-SRAM cell

IV. STABILITY ANALYSIS OF THE PROPOSED CELL

The stability of the SRAM cell is of equal importance to that of power consumption. Hence the stability of the proposed cell is measured and compared with the stability of the conventional 6T-SRAM cell. There are two widely used techniques to measure the stability of the cell. Those are the Static noise margin method (SNM) [7] and the N-Curve [8,9] method. The drawback of SNM method is the absence of an inline tester [10]. Hence for SNM calculation some extra mathematical effort has to be given to find the largest possible embedded square in the eye of the butterfly diagram. The N-Curve is a simple technique which finds the stability of the cell easily.

The four important N-Curve parameters in the in the SRAM cell are SVNM, SINM, WTV, WTI. Static Voltage Noise Margin (SVNM) is the voltage difference between the first and second zero crossing of the N-Curve. It is the maximum DC voltage which can be tolerated at the input of the cell before changing its state. Static Current Noise Margin (SINM) is the maximum DC current which can be injected at the input of SRAM cell before changing its state. It is measured as the maximum current value in the curve between the first and second zero-crossing. Write trip voltage is the voltage needed before flipping the internal node. It is measured as the difference between the second and third zero crossing of the N-Curve. Write trip current is the amount of input current which writes the cell when both the bit lines are kept at V_{dd} . It is the peak value of the input current between the second and third zero-crossing [10].

A stable SRAM cell must have high SVNM and high SINM. So SPNM which is the product of SVNM and SINM must be high for a high stable cell. WTV and absolute value of WTI should be small for a better writable cell. Hence WTP, the product of WTV and WTI should be smaller for a better writable cell [8].



Different Cells	Average Power	SVNM	SINM	SPNM	WTV	WTI	WTP
6T-SRAM	78.12nW	335.878mV	42.7472µA	7.322µW	517.714mV	13.953µA	5.044µW
LCR-SRAM	58.57nW	320.811mV	34.2643µA	5.588µW	524.77mV	9.448µA	3.251µW
Increment (%)	25.0256	4.486	19.844	23.682	-1.363	32.287	35.547
Comment	Improve	Degrade	Degrade	Degrade	Improve	Improve	Improve

Table 1: Comparison of LCR-SRAM cell vs 6T-SRAM cell

Figure 8 shows the N-Curve for the proposed LCR-SRAM cell. The SVNM, SINM, WTV, WTI are calculated from the zero-crossing of the curves and tabulated in table 1. The SPNM is found by integrating the plot from first to second zero-crossing. The WTP is found by integrating the plot from second to third zero-crossing. The SPNM and the WTP values are also tabulated in table 1. Figure 9 shows the N-Curve analysis for the conventional 6-T SRAM cell. All the above six parameters are calculated in the similar fashion; tabulated in table 1 and the stability of the proposed cell is compared with respect to it.



V. CONCLUSION

A novel LCR-SRAM cell is designed using GPDK-90 nm technology library. The cell is designed using eight transistors. From the simulation result it is found that the power consumption is reduced by 25.02%. As the stability and the write ability of the cell is also the important parameter of the cell they are also calculated using N-Curve method. The SPNM of the proposed cell is found to be degraded by 23% than the conventional 6-T SRAM cell whereas the WTP increases by 35%. This indicates that the proposed LCR-SRAM cell is more writable and consumes less power than the conventional 6-T SRAM cell though the stability reduces a little bit.

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