An analytical subthreshold surface potential model for a short-channel dual-metal-gate (DMG) recessed-source/ drain (Re-S/D) SOI MOSFET

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***Abstract*— In this paper, an analytical subthreshold surface potential model is presented for a short-channel dual-metal-gate (DMG) recessed-source/drain (Re-S/D) silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect-transistor (MOSFET). The model has been developed by solving the 2D Poisson's equations in the channel region with appropriate boundary conditions assuming a parabolic potential profile in the transverse direction of the channel. The developed model is analyzed extensively for a variety of device parameters like the oxide thickness, silicon and buried oxide (BOX) thicknesses, thickness of the source/drain extension in the BOX, control and screen gate length ratio and different combination of metal work function of control and screen gates. The validity of the present analytical model is verified with ATLAS™, a 2D device simulator from SILVACO Inc.**

Index Terms— DMG FD SOI MOSFETs, recessed-source/drain (Re-S/D). Short Channel Effects.

I. INTRODUCTION

The continuing growth in VLSI industry shifts technology from silicon to Silicon-on-Insulator (SOI) for getting better performances like higher circuit speed [1], [2], less threshold voltage roll-off [3], lower power consumption [4], attenuated short channel effects and compatibility with existing IC fabrication process [5]. Further, the ultra-thin-body (UTB) fully-depleted SOI MOSFET is a structure which is ultra-scalable because it inherits the benefits of SOI technology even at extremely shorter channel length [6].

However, due to the ultra-thin source and drain regions, fully depleted (FD) SOI MOSFETs possess large series resistance which leads to the poor current drive capability of the device, despite having excellent short-channel characteristics [7]. The recessed-source/drain (Re-S/D) UTB SOI MOSFET was proposed and fabricated by Zhang et al. [8] to overcome this large series resistance problem. In the Re-S/D UTB SOI MOSFETs, source and drain regions are extended deeper into the buried oxide (BOX) to minimize their resistance contribution in total series resistance of the device. Svilicic et al. presented an extensive analysis of this phenomenon by developing a short-channel threshold voltage model for Re-S/D UTB SOI MOSFETs [9]. The concept of dual-metal-gate (DMG) structure [10- 12] is has already been adopted in Re-S/D UTB SOI MOSFETs to include its implicit advantages. The DMG Re-S/D UTB SOI MOSFET device has higher on-current density, lower Drain Induced Barrier Lowering (DIBL) and reduced hot carrier effects (HCE). In the present work, to get the insight of subthreshold behaviour of DMG Re-S/D UTB SOI MOSFET, an analytical subthreshold surface potential model is developed and a thorough analysis is also carried out on the developed surface potential model by varying device parameters like the oxide, silicon and buried oxide (BOX) thickness, thickness of source/drain extension in the BOX, control and screen gate length ratio and different combination of metal work function of control and screen gate.

II. DEVICE STRUCTURE

Fig. 1 shows the cross-section of a short-channel DMG recessed Re-S/D SOI MOSFET. The position along the channel length is represented by the x- axis whereas the channel depth is represented by the y- axis as shown in the figure. The metal strips (φ_{M1} and φ_{M2}) divide the entire channel into two different virtual regions with potential distribution as $\phi_1(x,y)$ and $\phi_2(x,y)$ where L_1 and L_2 are their respective lengths connected in a non-overlapping way.

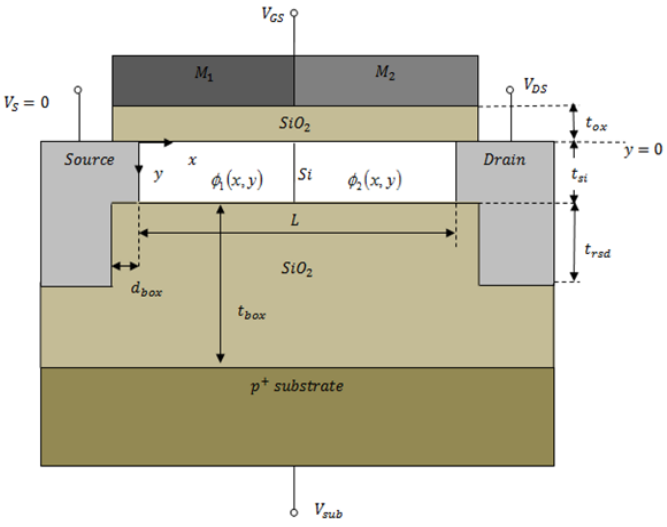

Fig. 1: Cross sectional view of DMG-FD-R- S/D on SOI MOSFET.

The symbols t_{Si}, t_{ox}, t_{box} and t_{rsd} represent the thicknesses of the silicon, gate oxide, buried oxide and the depth of S/D in the buried oxide. d_{box} is the length of the source/drain overlap over the buried-oxide. The device is assumed to be doped uniformly having source/drain and body regions with doping densities of N_d and N_a respectively. The source/drain to channel junction is assumed to be abrupt. The MOSFET is biased by gate voltage of V_{GS}, drain voltage of V_{DS} and substrate voltage V_{sub} keeping the source voltage $V_S = 0$.

III. Surface Potential Model

The potential distribution $\phi_i(x,y)$ in the channel is obtained by solving the following 2D Poisson's equation

$$\frac{\partial^2 \phi_i(x,y)}{\partial x^2} + \frac{\partial^2 \phi_i(x,y)}{\partial y^2} = \frac{qN_a}{\varepsilon_{Si}} \tag{1}$$

where $i = 1, 2$ denotes the respective channel regions under metal strip 1 and 2; N_a is the effective body doping concentration; q is the electronic charge and ε_{Si} being the permittivity of Silicon. The potential distributions in the two regions are approximated by following parabolic functions

$$\phi_i(x,y) = \phi_{si}(x) + C_{i1}(x)y + C_{i2}(x)y^2 \tag{2}$$

The coefficients C_{i1} and C_{i2} are function of x only. These coefficients are derived using the appropriate boundary conditions [10]. The symbol ϕ_{si} represents the potential at SiO_2/Si interface.

Solving Eqn. (1) at channel/SiO_2 and channel/ BOX interfaces with proper boundary conditions [10] yields following differential equations for front- and back- surface potentials;

$$\frac{\partial^2 \phi_{si}(x)}{\partial x^2} - \alpha_s \phi_{si}(x) = \beta_{s_i} \tag{3}$$

$$\frac{\partial^2 \phi_{bi}(x)}{\partial x^2} - \alpha_b \phi_{bi}(x) = \beta_{b_i} \tag{4}$$

where, $\phi_{si}(x)$ and $\phi_{bi}(x)$ are surface potential at channel/SiO_2 and channel/ BOX interfaces, respectively. α_s, β_{s_i}, α_b and β_{b_i} are constants which are determined from boundary conditions[10].

Now the solution of Eqns. (3) and (4) gives following expressions for front and back surface potentials

$$\phi_{s1}(x) = \frac{\psi_{f,d1}\sinh(\lambda_f x) - \psi_{f,s1}\sinh(\lambda_f (x - L_1))}{\sinh(\lambda_f L_1)} - \sigma_{f1} \tag{5}$$

$$\phi_{s2}(x) = \frac{\psi_{f,d2}\sinh(\lambda_f (x - L_1)) - \psi_{f,s2}\sinh(\lambda_f (x - L))}{\sinh(\lambda_f L_2)} - \sigma_{f2} \tag{6}$$

$$\phi_{b1}(x) = \frac{\psi_{b,d1}\sinh(\lambda_b x) - \psi_{b,s1}\sinh(\lambda_b (x - L_1))}{\sinh(\lambda_b L_1)} - \sigma_{b1} \tag{7}$$

$$\phi_{b2}(x) = \frac{\psi_{b,d2}\sinh(\lambda_b (x - L_1)) - \psi_{b,s2}\sinh(\lambda_b (x - L))}{\sinh(\lambda_b L_2)} - \sigma_{b2} \tag{8}$$

where, σ_{f1}, σ_{f2}, σ_{b1}, σ_{b2} $\psi_{f,s1}$, $\psi_{f,s2}$, $\psi_{f,d1}$, $\psi_{f,d2}$, $\psi_{b,s1}$, $\psi_{b,s2}$, $\psi_{b,d1}$, $\psi_{b,d2}$ are constants and determined from suitable boundary conditions [10]. Symbols λ_f and λ_b are the characteristic length associated with the front gate surface potential and back gate surface potential, respectively.

IV. Results and Discussion

The numerical simulations have been carried out by a two-dimensional (2D) device simulator ATLAS™ from Silvaco Int. [13], for obtaining surface potential profile. The drift-diffusion model has been employed during simulation. For velocity saturation in high field, FLDMOB mobility model has been used in which the velocity saturation depends on the parallel electric field in the direction of current flow. Moreover, the CVT mobility model has also been used as it is a complete mobility model in which the mobility depends on doping density, temperature, parallel electric field and vertical electric field. The FERMI carrier statistical model is used to reduce carrier concentrations in heavily doped regions. The source-body and the drain-body junctions are abrupt in nature. The taken metal work-function of the control gate is $\phi_{M1} = 4.8$ eV (Au: Gold) while for screen gate various metals are taken with work function $\phi_{M2} = 4.8\,\text{eV}, 4.6\,\text{eV}$ and $4.4\,\text{eV}$.

Fig. 2 displays surface potential profile along the channel length at channel/SiO_2 and channel/BOX interfaces for. $t_{rsd} = 30\text{nm}$. It is seen that the inversion layer form's at the back channel first before the onset of the front-gate inversion which may be attributed to the fact that back channel minimum surface potential is more than that of front channel minimum surface potential.

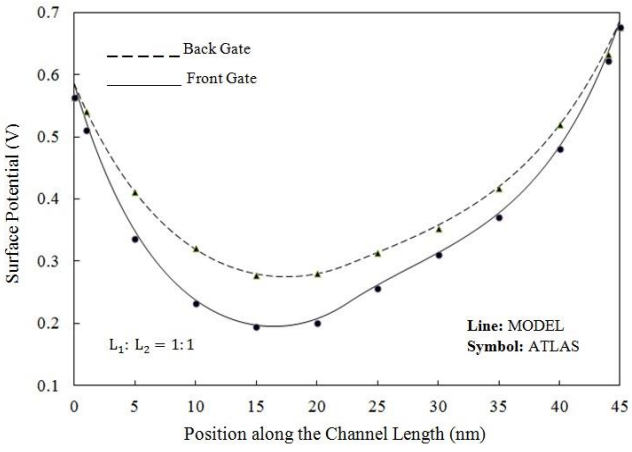

Fig. 2 Surface Potential along the channel length at front and back gates. where φ_{M1} =4.8, φ_{M2} =4.6, N_a =10^{15} cm^{-3}, N_d =10^{20}cm^{-3}, t_{ox} =2nm, t_{si} =10nm, t_{box} =200nm, t_{rsd} =30nm, V_{GS} =0.1V, V_{DS} =0.1V

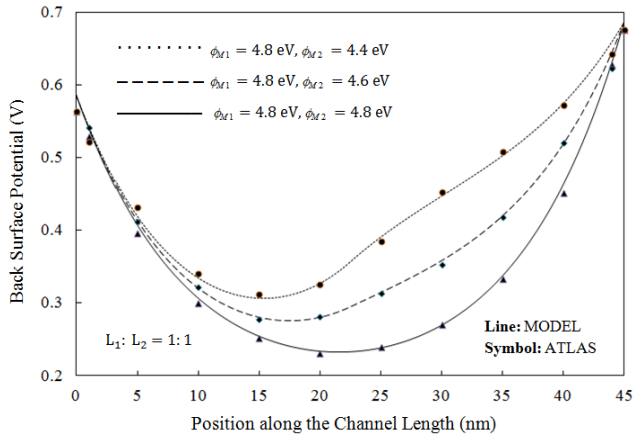

Fig. 3 Back Surface Potential along the channel at different control to screen work function combinations. Where N_a =10^{15}cm^{-3}, N_d =10^{20}cm^{-3}, t_{si} =10nm, t_{ox} =2nm, t_{box} =200nm, t_{rsd} =30nm, V_{GS} =0.1V, V_{DS} =0.1V

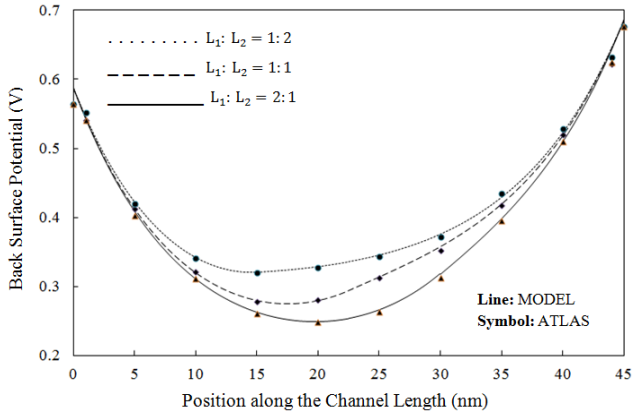

Fig. 4 Back Surface Potential along the channel at different control to screen gate length ratio. where φ_{M1} =4.8, φ_{M2} =4.6, N_a =10^{15} cm^{-3}, N_d =10^{20}cm^{-3}, t_{si} =10nm, t_{ox} =2nm, t_{box} =200nm, t_{rsd} =30nm, V_{GS} =0.1V, V_{DS} =0.1V

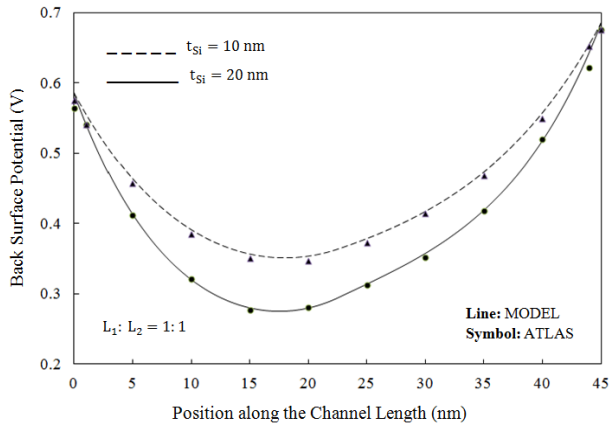

Fig. 5 Back Surface Potential versus Gate length for varying Si film thickness. where φ_{M1} =4.8, φ_{M2} =4.6, N_a =10^{15} cm^{-3}, N_d =10^{20}cm^{-3}, t_{ox} =2nm, t_{box} =200nm, t_{rsd} =30nm, V_{GS} =0.1V, V_{DS} =0.1V

So the back channel is responsible for the smaller threshold voltage of the device. It should be noted that for t_{rsd} > 3nm the back channel dominates over the front one and hence for the rest of analysis the back surface potential (at channel/BOX interface) is considered.

Fig. 3 shows back surface potential along the channel length at different control to screen gate work function combinations. It is seen that at the decreased work function of the screen gate, the minimum surface potential is found to be higher, and back surface potential exhibits a step function in the surface potential along the channel. This step profile at the junction of two gate metal electrodes screens the region near the drain end from the variations in the drain voltage.

Fig. 4 depicts back surface potential along the channel length at varying control to screen gate length ratio keeping the total channel length to a constant value. It is found that the device with a higher length of screen gate will have higher minimum surface potential and lower source-channel barrier height. Also, it is found that at higher length of screen gate minimum surface potential goes closer to the source and hence it is less prone to the drain voltage variations as a result lesser DIBL is observed in the device.

Fig. 5 demonstrates back surface potential along the channel length at varying channel thickness. It is concluded that as the channel thickness increases, the minimum surface potential decreases, increasing the potential barrier between the channel and the source.

The plot in Fig. 6 displays back surface potential along the channel length at varying buried oxide thickness. It is found that for thicker buried oxide, the minimum surface potential decreases.

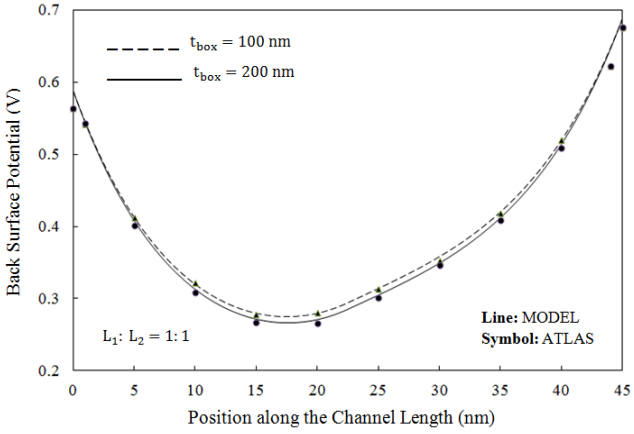

Fig. 6 Back Surface Potential versus Gate length for varying buried oxide thickness. where φ_{M1} =4.8, φ_{M2} =4.6, N_a =10^{15}cm^{-3}, N_d =10^{20}cm^{-3}, t_{si} =10nm, t_{ox} =2nm, t_{rsd} =30nm, V_{GS} =0.1V, V_{DS} =0.1V.

The back surface potential along the channel length at varying oxide thickness is shown in Fig. 7. It is observed that as the buried oxide thickness increases, the minimum surface potential decreases.

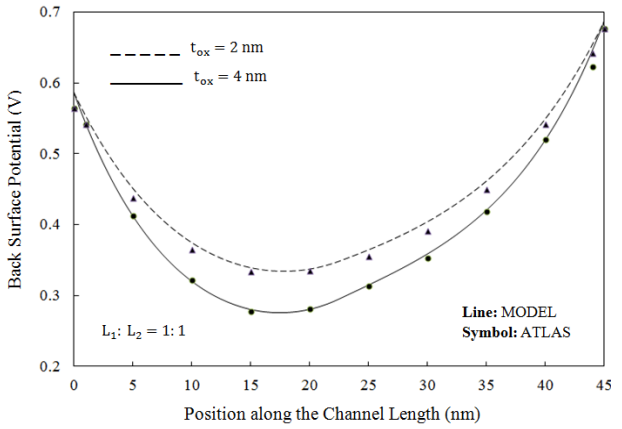

Fig. 7 Back Surface Potential versus Gate length for varying oxide thickness. where φ_{M1} =4.8, φ_{M2} =4.6, N_a =10^{15} cm^{-3}, N_d =$10^{20}cm^{-3}$, t_{si} =10nm, t_{box} =200nm, t_{rsd} =30nm, V_{GS} =0.1V, V_{DS} =0.1V

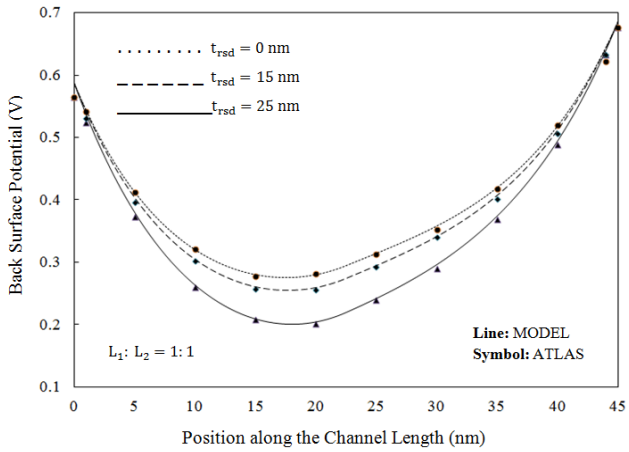

Fig. 8 Back Surface Potential versus Gate length for depth of S/D in the buried oxide. where φ_{M1} =4.8, φ_{M2} =4.6, N_a =10^{15} cm^{-3}, N_d =$10^{20}cm^{-3}$, t_{si} =10nm, t_{ox} =2nm, t_{box} =200nm, V_{GS} =0.1V, V_{DS} =0.1V

Fig. 8 exhibits back surface potential along the channel length at different penetration of source/drain in the BOX. It is seen that as the source/drain penetration increases, the minimum surface potential decreases, increasing the potential barrier height between the channel and the source.

V. Conclusion

A two-dimensional subthreshold surface potential model is developed for a fully-depleted recessed-source/drain (Re-S/D) DMG SOI MOSFET. The analytical results are compared with the simulated results obtained from ATLAS 2D device simulator and have been found in a good agreement. The developed analytical model confirms the ability of a DMG structure in a UTB recessed S/D SOI MOSFET to overcome the HCEs and lowering DIBL which are rampant in an SOI MOSFET.

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