FPGA Implementation of Pipelined CORDIC Based Quadrature Direct Digital Synthesizer with Improved SFDR

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***Abstract*—Direct Digital Synthesizers (DDSs) or Numerically Controlled Oscillators (NCOs) are nowadays prominently used in the applications of RF signal processing, satellite communications, etc. This paper brings out the FPGA implementation of one such DDS which has quadrature outputs. The proposed design, which is based on pipelined CORDIC, has considerable improvement in terms of spurious free dynamic range (SFDR) compared to other existing designs at reduced hardware. The design is implemented on Xilinx XC3S500E-4FG320 FPGA, fabricated in 90 nm process technology. The design has utilized 487 slices and 967 4-input look up tables (LUTs) as its hardware count. The maximum sampling frequency of the proposed design is 107.216 MHz. The SFDR of proposed DDS is -96.31 dBc.**

***Index Terms*—CORDIC, DDS, NCO, Quadrature outputs, FPGA, SFDR.**

I. Introduction

FREQUENCY synthesizers, sometimes also called oscillators, are an essential unit of many communication systems. With the maturity of digital systems, communication systems are employing digital sub systems in their units, thus making the usage of digital systems more ubiquitous. Direct digital synthesizers (DDS) are a class of frequency synthesizers in digital domain, which generate waveforms of desired frequencies [1]. Sometimes also called numerically controlled oscillators (NCO), these generate waveforms like sine, cosine, triangular, square or rectangular, saw tooth, etc. As mentioned earlier, these have wide applications in satellite communication systems, RF signal processing, etc. Many communication systems require quadrature inputs, for example both sine and cosine, for their systems thus bringing in the need of design of DDS which can generate quadrature outputs.

DDS offers many advantages over analog oscillators such as extremely precise tuning resolution of the output frequency, fast hopping of phase which reduces phase related errors, remotely controllable, better match of quadrature outputs when required, etc.

The phase to amplitude block of DDS, which will be described clearly in section II, decides the nature of output of the synthesizer. The construction of such block in the proposed design is done based on pipelined CORDIC, thus generating quadrature outputs, as it has an ability to generate both sine and cosine waves at a time. Other methods such as look up table method also exist in constructing the phase to amplitude conversion blocks in designing DDS.

CORDIC, stands for Coordinate Rotation DIgital Computer, has the capability of calculating values of many functions such as trigonometric, hyperbolic, arithmetic (multiplication and division), vector rotation, logarithmic, transcendental, etc. [2] – [3]. The coordinate system and mode of CORDIC is a choice to designers depending upon which application they want to implement.

The mode of CORDIC implemented in design of DDS' phase to amplitude block is rotation mode and the coordinate system used is circular coordinate system. The pipeline design of CORDIC facilitates in increasing the speed of calculation of outputs depending on the inputs given.

The rest of the paper is organised as follows. Section II briefly describes DDS, section III overviews CORDIC, section IV explains the proposed design methodology, section V shows the results of the proposed design and section VI concludes the paper.

II. Direct Digital Synthesizers

Direct digital frequency synthesis (DDFS) or DDS uses digital hardware blocks in generating arbitrary waveforms of different frequencies. The essential hardware blocks of a simple DDS are phase accumulator, phase to amplitude converter, digital to analog converter (DAC) and a low pass (reconstruction) filter. Figure 1 shows DDS in its simple form.

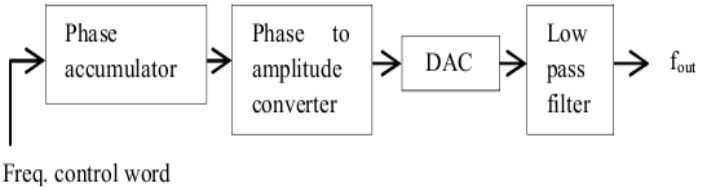

Fig. 1. A Direct Digital Synthesizer

The synthesizer unit has mainly two inputs, one being frequency control word and the other being system clock, many times used as sampling clock. It has got outputs based on desired number and frequency.

The first block, phase accumulator accumulates the phase at each clock cycle, depending on the required frequency of output waveform. The input to the block, being the frequency control word determines the output frequency. If the accumulator is of N

bit wide, and the period of the output wave being 2π rad, we can consider that $2^N = 2\pi$ rad. Let the sampling frequency of the system be F_s and the frequency of output is F_{out}. Depending on the required frequency (F_{out}), the step of accumulation is determined. It is determined using the following relation.

$$\Delta ACC = (F_{out} / F_s)* (2^N) \quad (1)$$

Where, ΔACC is step of accumulation. We can consider that the accumulator is a 2^N modulo adder. The output of accumulator, which is N bit wide, is fed into phase to amplitude converter that converts the input phase equivalent to output amplitude equivalent.

When $\Delta ACC = 1$, the phase accumulator accumulates with minimum accumulation step and the minimum frequency thus generated is given by

$$F_{out(min)} = F_s / 2^N \quad (2)$$

The maximum frequency the DDS can generate, without aliasing effects, is any how based on the Nyquist sampling theorem, and is given by

$$F_{out(max)} = F_s / 2 \quad (3)$$

In practice, $F_{out(max)}$ is considerably lower than the mentioned value in equation (3).

The second block of the DDS is called phase to amplitude converter. As the name suggests, this block generates the output waveform in the form of bit strings, depending on the requirement of the word length. There exist different methods of mapping from phase to amplitude. A number of methods are given for sine wave in [4]. These involve look up table (LUT) method, interpolation method, CORDIC based, etc. LUT methods require ROMs to store the phase amplitude equivalents of the wave. Many ROM based methods are discussed in [5]. One good method using analog interpolation is described in [6]. Of all methods, CORDIC based methods give better performance in terms of phase quantization noise and amplitude quantization noise.

The output of phase to amplitude converter is sent to DAC which converts digitally represented waveform to analog one. The size of DAC has to match with the size of digital output of phase to amplitude converter (PAC). Let the depth of phase input of PAC be M bits and depth of amplitude output be P bits. Here come the two performance parameters of the DDS, SFDR and signal to noise ratio (SNR).

SFDR is the ratio of strength of the desired fundamental signal to the strongest spurious signal present in the output. When the carrier level is assumed to be at 0 dB, the formula for maximum level of spurs is given by

$$S_{max} = - 6.02M + 3.92 \text{ dB} \quad (4)$$

Similarly, SNR is given by

$$SNR = - 6.02P – 1.76 \text{ dB} \quad (5)$$

Since the system being digital, quantization effects exist in phase information as well as amplitude information. It is observed that, SFDR is related to phase quantization and SNR is related to amplitude quantization. Observing equations (4) and (5) gives that M = P + 1. This means that spurs are caused not because of phase truncation, but because of amplitude quantization.

Several methods of improving SFDR are discussed in [7]. Since sine and cosine are of much interest now days, the methods to improve SFDR as well as SNR are being concentrated only on the above waveforms. Methods such as phase-dithering, noise-shaping, odd-number approach, etc. have shown considerable improvement in SFDR of the DDS.

III. Overview of CORDIC

CORDIC, as mentioned earlier, stands for Coordinate Rotation DIgital Computer. It computes the rotation of vectors using simple additions and shifts. The mode operated is either rotation mode or vectoring mode. CORDIC can operate either in circular coordinate system, or in linear coordinate system, or in hyperbolic coordinate system. The basic equation of CORDIC for i^{th} iteration is given below, which is for circular coordinate system and for rotation mode of operation.

$$\begin{aligned} X_{i+1} &= [X_i – C_i * Y_i * 2^{-i}] * K_i \\ Y_{i+1} &= [Y_i + C_i * X_i * 2^{-i}] * K_i \\ Z_{i+1} &= Z_i – C_i * \arctan(2^{-i}) \end{aligned} \quad (6)$$

C_i is the direction of rotation which has a value of either 1 or – 1 depending on whether the rotation is positive or negative. K_i is the scaling factor of ith iteration stage and it can to be computed at the end of all iterations since it comes out as a product of all stages. The theoretical value of K is given as

$$K = \pi_i \; K_i = 0.60725 \quad (7)$$

Many architectural designs are reviewed in [8] and [9] which makes designer to choose desired CORDIC architecture for his design.

Figure 2 shows the CORDIC stage for ith iteration.

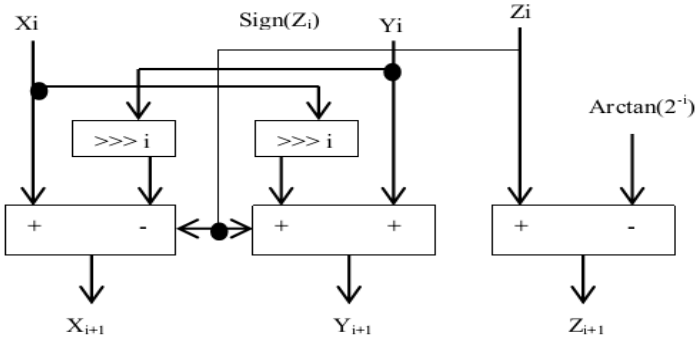

Fig. 2. CORDIC stage for ith iteration

Pipelined CORDIC [8], has advantage over other fully dedicated architectural CORDIC (FDA) since it improves the speed of operation and also gives out varying outputs at every clock cycle, for varying inputs. The ith iteration stage of pipelined CORDIC is similar in structure to that of one in FDA except that registers are used to store the input and output values of ith iteration. Figure 3 shows a stage of pipelined CORDIC. In designing dedicated pipelined architectures, one of either IN_REGS or OUT_REGS is eliminated to improve latency of the design.

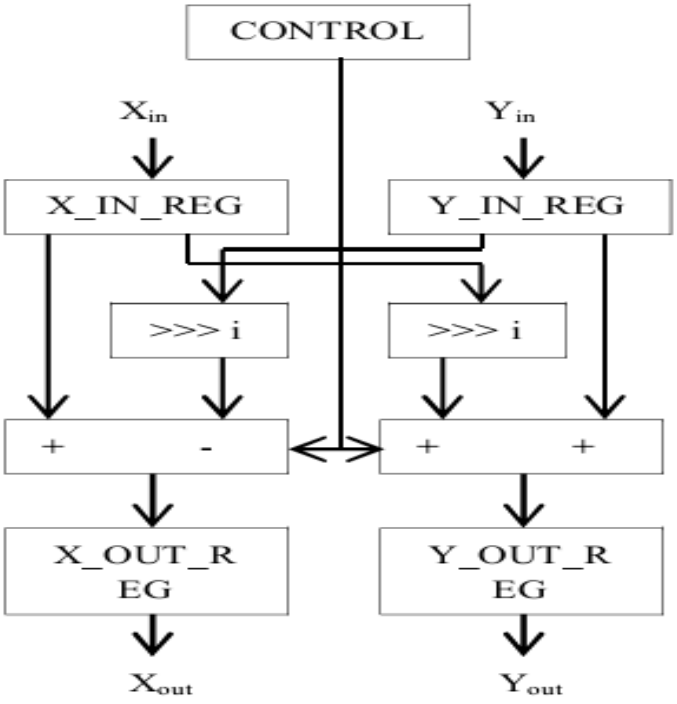

Fig. 3. Pipelined CORDIC stage for ith iteration

IV. Proposed Design of DDS

As mentioned earlier, the proposed design of DDS is based on pipelined CORDIC, which acts as phase to amplitude converter. The phase accumulator has a size of 18 bits, of which the most significant bit corresponds to the sign of the input, which is frequency control word. The output of phase accumulator is fed to mapped CORDIC block, which has a mapping mechanism that maps the pipelined CORDIC over the entire 2π range. Figure 4 shows the phase accumulator schematic of proposed design.

The output of the phase accumulator, which is of 18 bit wide, is given as phase input to the mapped CORDIC unit. The mapper mechanism maps the CORDIC unit over entire 2π range by utilizing first three most significant bits of the phase input. The CORDIC unit utilizes only 15 bits to compute the amplitude of the quadrature wave outputs. The method used to store arctan values inside the CORDIC unit makes the amplitude of the outputs very accurate, till 5 places after decimal point.

Figure 5 shows one stage of pipelined CORDIC of proposed design.

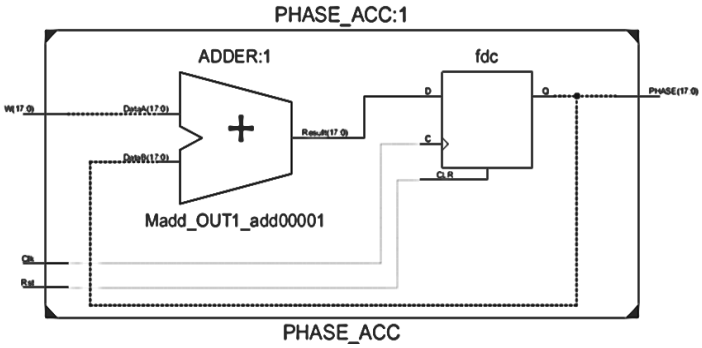

Fig. 4. Phase accumulator unit of proposed design

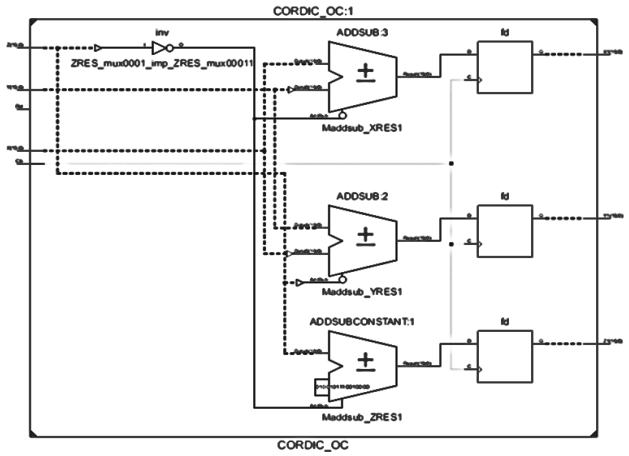

Fig. 5. A stage of pipelined CORDIC in proposed design

The shifting in intermediate stages in the proposed design is made hardwired, thus improving latency and reducing the delay of the design. The schematic of top module is shown in figure 6.

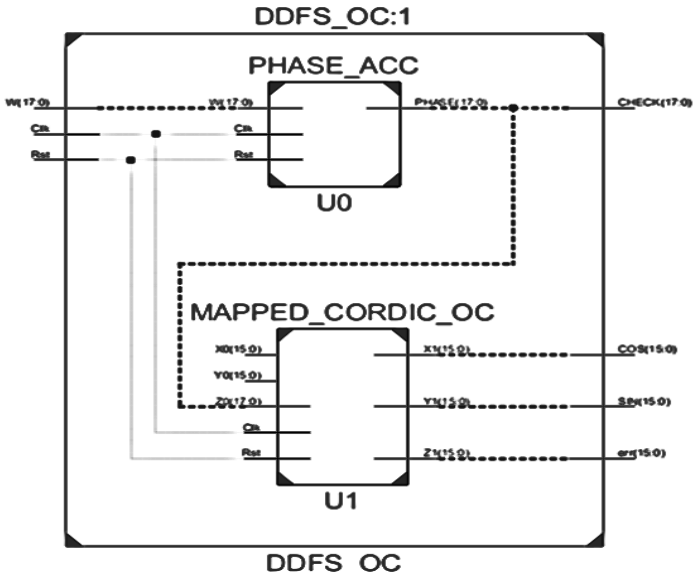

Fig. 6. Schematic of top module of proposed design

The check output of the top module ensures the correct increment of the accumulation step. In the proposed design, the

amplitude is represented using 16 bits. Thus, the total number of amplitude quantization levels is 2^{15} since the most significant bit represents the sign of the amplitude.

As seen from figure 6, there are two outputs of the proposed design corresponding to the quadrature outputs of sine and cosine. Thus, the proposed design generates quadrature outputs using single architecture. As a whole, the inputs and outputs of the proposed design are frequency control word for setting the output frequency, clock for setting sampling frequency, quadrature waves and check signal for checking accumulation index.

V. RESULTS

The proposed design is implemented using Xilinx XC3S500E-4FG320 FPGA. The software tools used are Xilinx XST for synthesis of the design and Modelsim for simulation verification. Table I shows the hardware utilization of the proposed design when implemented on Xilinx FPGA. Since the proposed design has been designed using pipelined CORDIC, the number of registers, in turn the number of flip flops required has increased.

TABLE I. DEVICE UTILIZATION SUMMARY OF PROPOSED DESIGN

LOGIC UTILIZATION	USED
Number of slices	487 (10%)
Number of slice flip flops	788 (8%)
Number of 4 input LUTs	967 (10%)

From the statistics in table I, the area constraint ratio of the design is 11 out of 100.

Figure 7 shows the ModelSim simulation that shows quadrature outputs of the proposed design.

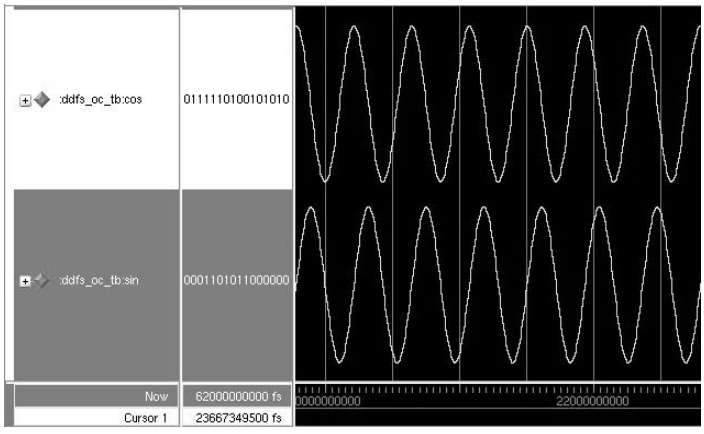

Fig 7. Quadrature outputs of proposed design in ModelSim

According to equation (4), the SFDR for the proposed design has to be - 94.2 dBc. But, the calculated value is – 96.31 dBc, thus proving the design better than other designs. Figure 8 shows the FFT power spectrum of the proposed DDS. Table II shows the comparison of proposed design with few existing designs.

TABLE II. COMPARISON TABLE OF PROPOSED DESIGN WITH EXISTING DESIGNS

CORDIC based DDFS	Madisetti [10]	Swartzlander [11]	Sung [12]	Proposed Design
Maximum sampling rate (MHz)	80.4	1018	100	107.216
SFDR (dBc)	81	90	84.4	96.31
Output Resolution (bits)	16	16	16	16

From the comparison in table, the proposed design is better in all aspects. However, the performance of the proposed design can be still improved if we carefully design the phase accumulator and CORDIC's angle data path.

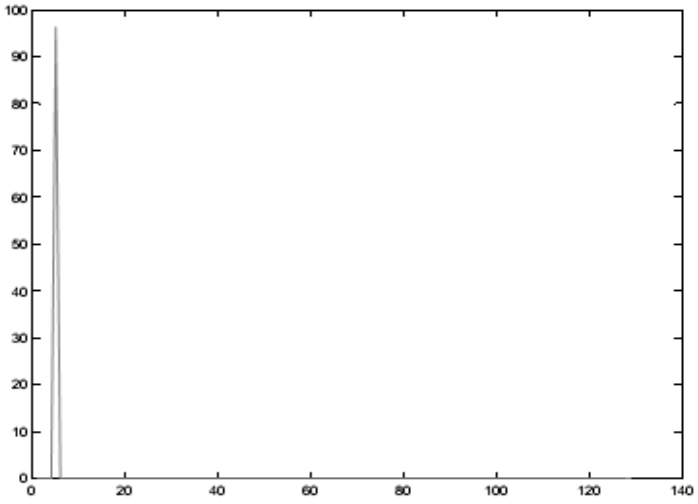

Fig. 8. FFT power spectrum of DDS to calculate SFDR

VI. CONCLUSIONS

This paper presents a design of DDS, which is also called a NCO. The proposed design is designed based on pipelined CORDIC unit used as phase to amplitude converter. The proposed design has a SFDR of – 96.31 dBc for 16 bit output amplitude resolution. In addition to that, the proposed design produces quadrature outputs which have better phase match thus making the design more useful for most of the communication systems. The simple design of DDS based on CORDIC always is a better choice since implementing this in circuits such as mixers, digital down/up converters is simpler in terms of hardware utilization. The higher the phase accumulator data width, the lesser is the phase quantization error. Hence, amplitude accuracy of the output waveforms is improved.

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