Improved Techniques for High Performance Noise-Tolerant Domino CMOS Logic Circuits

Srinivasa V S Sarma D and Kamala Kanta Mahapatra

Abstract—Dynamic CMOS gates are widely exploited in high-performance designs because of their speed. However, they suffer from high noise sensitivity. The main reason for this is the sub-threshold leakage current flowing through the evaluation network. This problem becomes more and more severe with continuous scaling of the technology. A new circuit technique for increasing the noise tolerance of dynamic CMOS gates is designed. A comparison with previously reported schemes is presented. Simulations proved that, when 90 nm CMOS technology is used to realize wide fan-in gates, the proposed design technique can achieve the highest level of noise robustness.

Index Terms—Domino logic, leakage current, noise tolerance, power consumption.

I. INTRODUCTION

Owing to the aggressive scaling down of the technology to the deep sub-micrometer regime, noise immunity is becoming a very important issue in the design of VLSI chips. The term ‘noise’ in digital integrated circuits generally refers to any possible event that may cause the voltage at a node to vary from its nominal value. There are different sources of noise in deep-submicron circuits. They are mostly related to crosstalk, small variations of the nominal supply voltage value, charge sharing and leakage current. The leakage current is the most critical, since in digital circuits it exponentially increases with the continuous shrinking of the MOS transistor dimensions [1, 2]. In fact, in order to limit dynamic energy consumption, the supply voltage is reduced in each new technology node. At the same time, the threshold voltage ($V_{TH}$) of the MOS transistor is scaled down to assure high performance. As a consequence, the sub-threshold leakage current continually increases, since it is exponentially dependent on $-V_{TH}$. Furthermore, the continuous reduction of the gate oxide thickness causes an exponential increase of the gate leakage current because of the enhanced tunneling of the carriers through the oxide itself.

Together with the increase of transistor density, specific design styles have also been aggressively exploited in order to achieve high performance. Here, it is the case of the domino logic design style, which is faster than the static CMOS. Moreover, domino gates are more compact, especially when they have a wide fan-in. Wide fan-in domino gates are often employed in the critical path of high-performance chips, such as in general purpose microprocessors or digital signal processors. As an example, wide fan-in OR gates and MUXs are used in the design of high-performance register files.

Domino gates suffer from higher noise sensitivity than their static CMOS counterparts. This is because of their low switching threshold voltage, which is equal to the $V_{TH}$ of the pull-down NMOS devices. Noise immunity has become a great concern, especially in the design of high fan-in gates. This is because of the high number of transistors and circuit branches, which cause more possible paths for gate and sub-threshold leakage currents.

Several techniques have been proposed to reduce the leakage noise sensitivity of high fan-in footless domino gates [3-10]. All the existing techniques improve the noise robustness of domino gates at a significant cost in terms of delay or energy consumption. Moreover, the degradation in speed and the increase in energy dissipation seem to become more and more troublesome with continuous technological progresses.

In this paper, a new technique is proposed to increase the noise immunity of dynamic gates with minimal energy and delay penalties.

II. DIFFERENT HIGH-PERFORMANCE NOISE TOLERANT CIRCUIT TECHNIQUES

(A) Wide fan-in Domino OR gate-Footless scheme

In Fig. 1, a typical wide fan-in domino OR gate-footless scheme is depicted. The footless scheme is often exploited in high-performance circuits because the discharge of the dynamic node is faster and the capacitive load of the clock line is reduced. The operation of a domino gate is managed by the clock signal.
During precharge (CLK = ‘0’):

The pre-charging PMOS charges the dynamic node up to Vdd.

During Evaluation phase (CLK = ‘1’):

The dynamic node is no longer constantly connected to Vdd through the pre-charge PMOS. Only the keeper provides a connection to Vdd until OUT goes high. This event could be forced by the sub-threshold leakage currents. In fact, even with all the inputs low, the leakage currents flowing through the NMOS pull-down network (PDN) could discharge the dynamic node. This effect is enhanced if a noise voltage pulse occurs at one or more inputs.

The noise voltage impulse causes two main effects.

i. First of all, the sub-threshold leakage current through the pull down NMOS transistor exponentially increases with the gate-to-source voltage (VGS) variation. As a result, the dynamic node is forced to be wrongly discharged.

ii. The drain-to-gate voltage (VDG) decreases with VGS increasing, thus decrementing the drain-to-gate leakage current.

Unfortunately, the reduction of the gate leakage current is almost irrelevant if compared with the increase of the sub-threshold leakage current. In fact, the drain-to-gate leakage dependence on VDG is less remarkable than the impact of VGS on the sub-threshold leakage current. As a result, the presence of a noise impulse at one or more gate inputs enhances the discharging mechanism of the dynamic node.

Besides an input glitch, also a fluctuation of the voltage level of the ground network may cause a wrong discharge of the dynamic node during the evaluation phase. In fact, a negative voltage pulse occurring at the ground line would increase the VGS of the NMOS transistors inside the PDN. The sub-threshold current flowing from the dynamic node would be higher, thus enhancing the discharge of the dynamic node.

From the simulation result, the leakage current was found to be 25.49 n.a.

(B) Wide fan-in Domino OR gate-Footed scheme

In Wide fan-in Domino OR gate-footed schematic-Leakage current Simulation the leakage current was found to be 257 n.a.
Advantages:

(i) An NMOS transistor $M_n$ is inserted between the dynamic node and the PDN. Thus this technique will be referred to as the dynamic node-footed scheme.

(ii) Three static inverters and the PMOS transistor $M_t$ are exploited to properly turn $M_n$ on.

(iii) At the beginning of the evaluation phase, owing to the finite delay of the inverters-chain ($T_{delay}$), both the Clk and NCLK signals are high. During this time (the “Transparency Window”), the gate can elaborate the input signals and the dynamic node can be eventually discharged.
(iv) After the time Tdelay is elapsed, NCLK becomes low and Mn is turned off. In this condition, owing to the stack effect, the charge leakage from the dynamic node to ground is exponentially reduced and the noise immunity of the gate is increased.

(v) Like the diode-footed technique, also the dynamic node-footed scheme leads to a very low area overhead.

Disadvantages:

The increased capacitive load of the Clk line and the increased resistance of the discharging path for the dynamic node because of the presence of the extra transistor MN.

Impact of Tdelay:

Case (a): The longer the Tdelay, the wider the gate transparency window, the faster the gate and the lower the noise immunity.

Case (b): The smaller the Tdelay, the thicker the transparency window. This leads to a slower gate but also to greater noise robustness.

The three techniques described above reduce the leakage current flowing through the dynamic node by exploiting the stack effect. These approaches do not reduce the overall leakage current, but only the leakage current at the dynamic node that drives the final static inverter and is the critical node.

III. IMPROVED HIGH-PERFORMANCE NOISE TOLERANT CIRCUIT TECHNIQUES

(A) Improved Wide fan-in Domino OR gate-Footed scheme

This modified technique has been proposed to reduce the leakage noise sensitivity of high fan-in footed domino gates. All the existing techniques improve the noise robustness of domino gates at a significant cost in terms of delay or energy consumption.

To prove the efficiency of the proposed technique, the external NMOS transistor is inserted between the evaluation PDN network and footer transistor. The purpose is to reduce sub threshold leakage current that flows through evaluation PDN, thereby reducing the gate noise sensitivity. The modified circuit is designed and simulated.

From the simulation result, the leakage current was found to be 42 p.a.

Advantages:

Leakage current is reduced considerably.

Disadvantages:

Though the leakage current through evaluation PDN is reduced, the current through footer is again increased, i.e. the leakage current through footer is 122 µ.a.

Discharge of dynamic node is not so fast as previous technique (unmodified).
The modified version is not giving faithful results. Though the same modified logic is applied to this circuit also, it does not hold good in this case, since it does not possess footer transistor. Thus the discharging of dynamic node is fast enough without modification. If any transistor is added to this PDN, then it reduces the sources potential, thereby increasing sub threshold leakage current.

From the simulation result, the leakage current was found to be 266.9 n.a.

Drawbacks:

(i) Increased sub threshold leakage current.
(ii) The equivalent resistance of PDN network may increase.
(iii) Gate delay may be present.

Thus this modified network may be omitted.

(C) Improved Wide fan-in Domino OR gate-Dynamic node footed scheme

To avoid the capacitive loading problems, we go for this modified new technique. The following modified circuit fulfills our requirements. In spite of having few drawbacks, as a whole its results are better than most other techniques.

Fig. 15 Improved Wide fan-in Domino OR gate-Dynamic node footed schematic implementation.

Fig. 16 Improved Wide fan-in Domino OR gate-Dynamic node footed schematic simulation.

Modifications made:

i. Reduction of the Transparency window (Tdelay) so that greater the noise robustness.
ii. Insertion of NMOS transistor Mn between dynamic node and PDN.
iii. Reduction of the Transparency window (Tdelay) so that greater the noise robustness.
iv. Insertion of NMOS transistor Mn between dynamic node and PDN.

This modified circuit is simulated and corresponding simulation result is shown below. From the simulation result, the leakage current was found to be 21.45 n.a.

Advantages:

(i) High noise robustness.
(ii) Reduction of leakage current.
(iii) Low area over overhead.

Disadvantages:

(i) Increased capacitive load of Clk line and increased resistance of discharging path of dynamic node due to presence of Mn and NMOS-externally inserted transistor.
(ii) Series of inverters, Mn, NMOS-externally inserted transistor all these cause dynamic energy dissipation, even output does not change.

IV. COMPARISON RESULTS

Table 1 Leakage current, power dissipation comparisons among different techniques of Wide fan-in Domino OR gate.

<table>
<thead>
<tr>
<th>Circuit Technique</th>
<th>Leakage Current (in Amps)</th>
<th>Power Dissipation (in Watts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Foot-less</td>
<td>25.49 n</td>
<td>497.34 n</td>
</tr>
<tr>
<td>Footed</td>
<td>257 n</td>
<td>503.7 n</td>
</tr>
<tr>
<td>Dynamic node footed scheme</td>
<td>702 n</td>
<td>232 µ</td>
</tr>
</tbody>
</table>
Table 2 Leakage current, power dissipation comparisons between unmodified & improved techniques of wide-domino OR gate.

<table>
<thead>
<tr>
<th>Circuit Technique</th>
<th>Leakage Current (in Amps)</th>
<th>Power Dissipation (in Watts)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Un-modified</td>
<td>Improved</td>
</tr>
<tr>
<td>Footed</td>
<td>257 n</td>
<td>42 μ</td>
</tr>
<tr>
<td>Footless</td>
<td>25.49 n</td>
<td>266.9 n</td>
</tr>
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<td>Dynamic node footed</td>
<td>702 n</td>
<td>21.45 n</td>
</tr>
</tbody>
</table>

V. CONCLUSION

Domino CMOS logic circuit family finds a wide variety of applications in microprocessors, digital signal processors, and dynamic memory due to their high speed and low device count. Domino logic is a CMOS logic style obtained by adding a static inverter to the output of the basic dynamic gate circuit. In this paper High-performance noise-tolerant circuit techniques for CMOS dynamic logic are studied and corresponding Domino logic techniques have been designed & simulated. The results are studied. The advantages & disadvantages are also observed. Few modifications have also been made to already existing domino techniques to get desired results. The improved techniques, though they suffer from few drawbacks, are giving better results compared with previous techniques.

Different Domino logic circuits are simulated in both Cadence virtuoso and Mentor graphics environments. The performance parameters of improved techniques are also compared with other standard architectures of Domino logic.

VI. REFERENCES