Design of a Novel Current Starved VCO via Constrained Geometric Programming

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***Abstract*— Presently the design of the optimal analog and mixed signal (AMS) circuits with lesser design cycle time is a great challenge for the designers. This paper describes the optimization of the current starved voltage controlled oscillator (CSVCO) circuit. The objective functions and constraints of the CSVCO circuit are in the form of posynomial functions of the design variables. The convex optimization and geometric programming method can well express the posynomial functions. In this work a novel current starved voltage controlled oscillator is designed by using geometric programming. Geometric programming is an efficient optimization technique in which the problem can be formulated as a convex optimization problem to obtain the global optimal solution for the given constraints with lesser design cycle time. The centre frequency of the VCO before and after optimization is 1.012GHz and 1.0000457GHz respectively. After optimization the frequency deviation of the circuit is reduced to .00457% from 1.2%. With this frequency precision the area is also minimized by the geometric programming method.**

***Keywords*— Design cycle, current starved voltage controlled oscillator (CSVCO), convex optimization, geometric programming, analog and mixed signal (AMS) circuit.**

I. INTRODUCTION

The complexity of the analog and mixed signal(AMS) circuit is increasing day by day and it is very difficult to design the optimized circuits with the desired specification in a lesser design cycle time. The optimization of the AMS circuit is necessary to achieve the better performance. The performance measures of any circuit are mainly depends upon the design parameters e.g. transistor sizing, bias current and other component values. The VCO design problem we considered in this paper is to determine the values of the design parameters that optimize the objective measure while satisfying some specifications or constraints. This design problem can be carried out by hand or some other computer aided design tool. In this paper we have carried out the optimization of the current starved voltage controlled oscillator (CSVCO) circuit by using the convex optimization [1]. The centre frequency of oscillation of current starved VCO is constrained to suffer from minimum deviation. The optimization is mainly focused on the sizing of the transistors in the circuit to meet the targeted oscillation frequency. Geometric programming is a special type of optimization technique in which the problem can be formulated as a convex optimization problem to obtain the global solution [2]. In this work we have used this convex optimization and geometric programming technique to achieve the 1GHz center frequency. The remaining part of the paper is organized as follows. Section II describes about the geometric programming. Section III of this paper elaborates the design of the VCO circuit. In section IV the design and synthesis environment has been outlined. The results of simulation study are discussed in section V. Finally the finding of the study has been concluded in section VI.

II. GEOMETRIC PROGRAMMING

Mainly optimization techniques are applied for selection of component values and transistor sizing. Geometric programming is a special type of optimization technique in which all the objective must be convex. Before applying this technique it has to confirm that whether the given problem is convex optimization problem or not. Convex optimization problem means the problem of minimizing a convex function subject to convex inequality constraints and linear equality constraints. A real valued function $f(x)$ defined on an interval (space) is called convex [3] if

$$f(tx_1 + (1-t)x_2) \leq tf(x_1) + (1-t)f(x_2)$$

For every $t, 0 < t < 1$ and $x_1 \neq x_2$

In the Fig.1 function $f(x)$ is represented as a convex function on an interval.

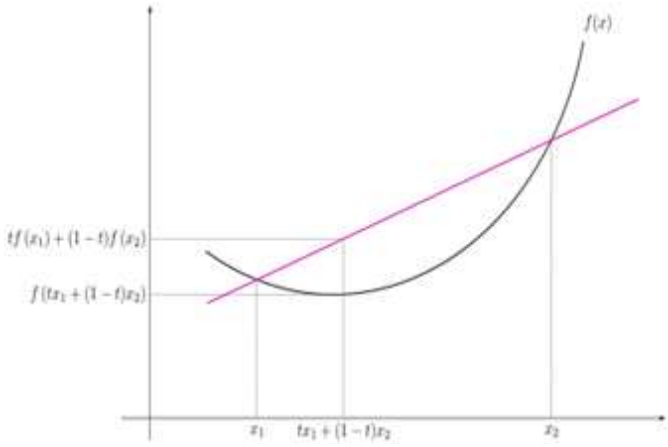

Fig.1.Convex function on an interval [3]

The convex optimization problem is in the form of minimize $f_0(x)$

Subjected to $f_i(x) \leq 1$, i=1, 2, 3…, m

$g_i(x) = 1$, i=1, 2, 3…, p
$x_i > 1$, i=1, 2, 3…, n

Where $f_i(x)$ is a posynomial function
$g_i(x)$ is a monomial function

In IC integration convex optimization and geometric programming has become a more efficient computational tool for optimization purpose [4]. This method has an ability to handle thousands of variables and constraints and solve efficiently. The main advantage of convex optimization technique is that it gives the global optimized value and the robust design [5]. The fact that geometric programs can be solved very efficiently has a number of practical consequences. For example, the method can be used to simultaneously optimize the design of a large number of circuits in a single large mixed-mode integrated circuit. In this case, the designs of the individual circuits are coupled by constraints on total power and area, and by various parameters that affect the circuit coupling such as input capacitance, output resistance, etc. Another application is to use the efficiency to obtain *robust designs* [2], [5] i.e., designs that are guaranteed to meet a set of specifications over a variety of processes or technology parameter values. This is done by simply replicating the specifications with a (possibly large) number of representative process parameters, which is practical only because geometric programs with thousands of constraints are readily solved.

In this work we have used the geometric programming technique to find out the optimized scaling ratio of the different stages in CSVCO to meet the desired center frequency with lesser deviation. Let x_i is the scaling ration of the i[th] stage, C_L is the load capacitance, and D is the total delay of the inverter stages then optimization problem is in the form of

Minimize sum (x_i)
Subjected to $C_L \leq C_{Lmax}$
$D \leq D_{max}$
Where C_{Lmax} and D_{max} are required design parameters and has a constant value.

III. DESIGN OF THE VCO CIRCUIT

The most popular type of the VCO circuit is the current starved voltage controlled oscillator. In this circuit the number of inverter stages is fixed with 5. The simplified view of a single stage current starved oscillator is shown in the Fig.2. Transistors M2 and M3 operate as an inverter while M1 and M4 operate as current sources. The current sources, Ml and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for current. The desired center frequency of the designed circuit is 1GHz with a supply of 1.8V. The CSVCO is designed both in usual manner as mentioned in [7], [8] and also by using geometric programming. In the traditional manner the design of the inverter stages in CSVCO are carried out to give a delay of 100ps. The length of all the transistors is fixed with 100nm. The design parameters of the VCO circuit are listed in the Table1. The general circuit diagram of the current starved voltage controlled oscillator is shown in the Fig.3. The oscillation frequency of the current-starved VCO for N of stages is given by [6], [7].

$$f_{osc} = \frac{I_D}{NC_{tot}V_{DD}} \quad (1)$$

Where $I_D = I_{D3} = I_{D4}$
N is the number of stages
C_{tot} is the total capacitance
V_{DD} is the supply voltage

The total capacitance C_{tot} is given by

$$C_{tot} = \frac{5}{2}C_{ox}(L_pW_p + L_nW_n) \quad (2)$$

Where C_{ox} is the oxide capacitance.

If the input control voltage of the CSVCO is VDD/2 then the oscillation frequency is given by

$$f_{center} = \frac{2I_{Dcenter}}{NC_{tot}V_{DD}} \quad (3)$$

The gain of the VCO [4] is given by

$$K_{VCO} = \frac{f_{max}-f_{min}}{V_{max}-V_{min}} \quad Hz/V \quad (4)$$

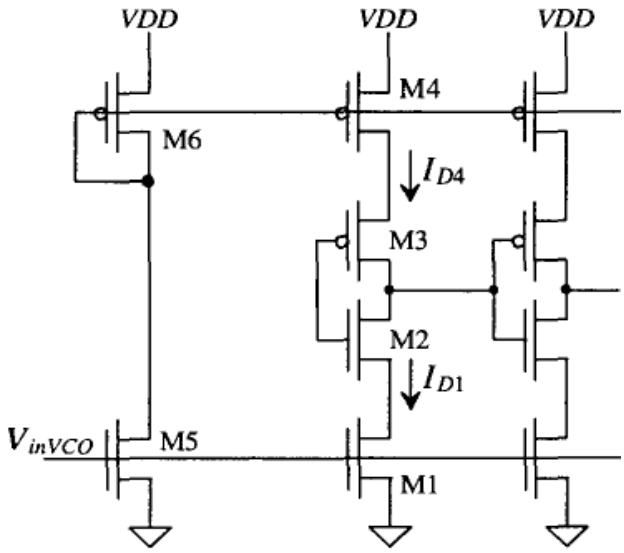

Fig.2.Simplified view of a current starved VCO [7]

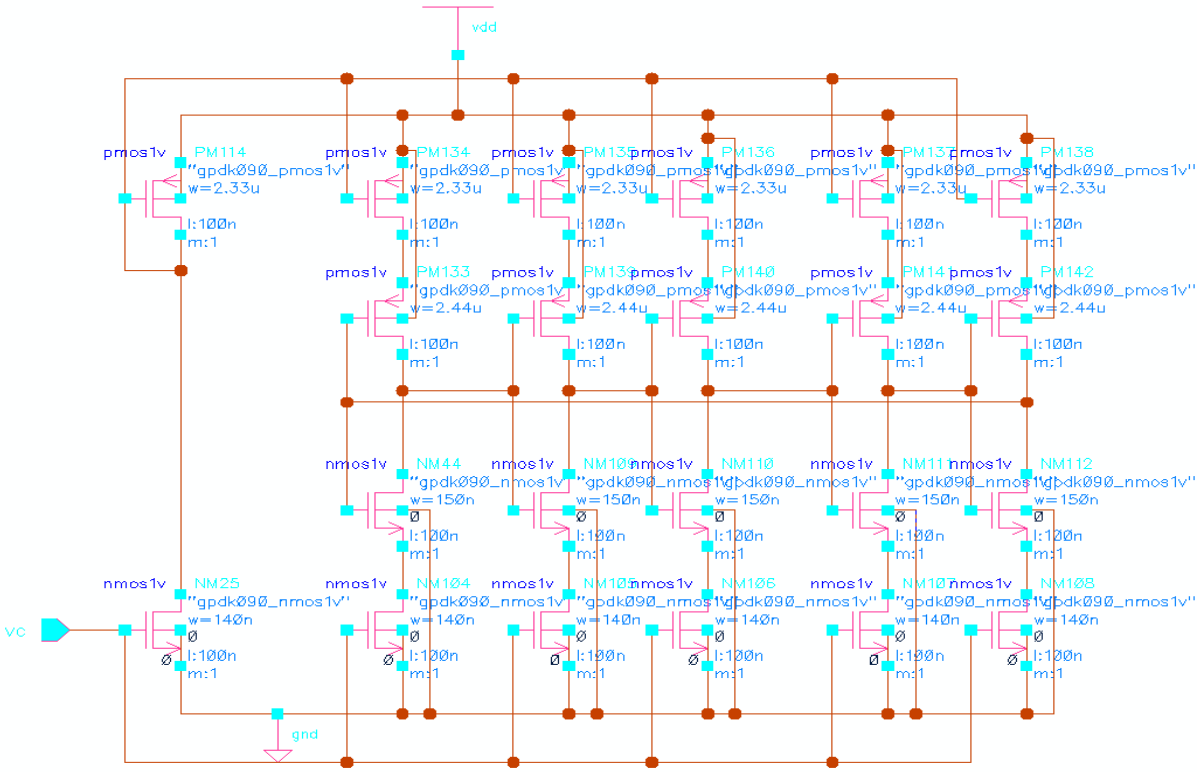

Fig.3.Circuit diagram of a 5 stage CSVCO

In the present work the sizing and scaling of the transistors M2,M3, current starved NMOS (M1) and PMOS (M4) of all stages in the CSVCO is carried out by geometric programming method as found in [1].

Table 1
List of design parameters of the CSVCO circuit for traditional method

Parameter	Value
Width of Current starved PMOS(W_{PCS})	2.33µm
Width of Current Starved NMOS(W_{nCS})	140nm
Width of PMOS in Inverter(W_P)	2.44µm
Width of NMOS in Inverter(W_n)	150nm
$L_{PCS} = L_{nCS} = L_P = L_n = L$	100nm

IV. SIMULATION ENVIRONMENT

The design entry of the circuits is carried out in the CADENCE Analog Virtuoso Environment using gpdk090 library. For performance analysis these circuits are simulated in the Spectre simulator of CADENCE tool. The optimized scale factor for transistor sizing is found out using the MATLAB environment.

V. RESULTS AND DISCUSSION

The simulation result for the scaling factors of the transistors in the inverter stages which are found out from the MATLAB are 1, 1, 1, 1, and 1.4058. The simulation graph for these results is shown in the Fig.4.

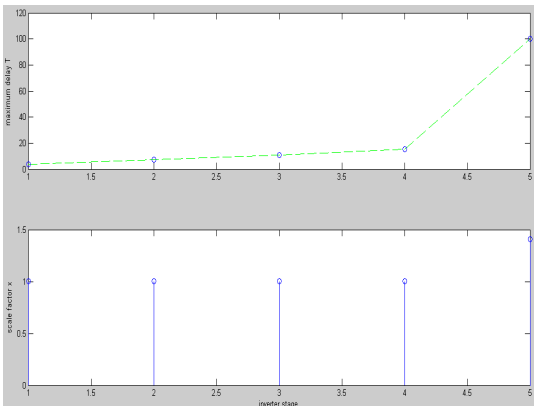

Fig.4.Scaling factors for different inverter stages of CSVCO

Then the transistor sizes are modified according to the scaling ratio. Since the scaling factor of all the stages are 1 except 5th stage, so the transistor sizing of the 5th stage only changed to get the better frequency precision. The sizes of the transistors of CSVCO optimized using convex optimization technique are listed out in the Table 2. Before optimization the centre frequency of the oscillation is found out 1.012GHz. And after applying the convex optimization and geometric programming to this circuit we got 1000.0457MHz. So the frequency deviation from its centre frequency is reduced to .00457% from 1.2%. The performance of both traditional and geometric programming is compared in the Table 3. The control voltage versus oscillating frequency characteristics of the CSVCO circuit is shown in the Fig.5.

Table 2
The transistor sizes of CSVCO using geometric programming method

Stage	Parameter	value
1	W_{PCS}	2.33µm
	W_{nCS}	140nm
	W_P	2.44µm
	W_n	150nm
2	W_{PCS}	2.33µm
	W_{nCS}	140nm
	W_P	2.44µm
	W_n	150nm
3	W_{PCS}	2.33µm
	W_{nCS}	140nm
	W_P	2.44µm
	W_n	150nm
4	W_{PCS}	2.33µm
	W_{nCS}	140nm
	W_P	2.44µm
	W_n	150nm
5	W_{PCS}	3.28µm
	W_{nCS}	195nm
	W_P	3.435µm
	W_n	215nm

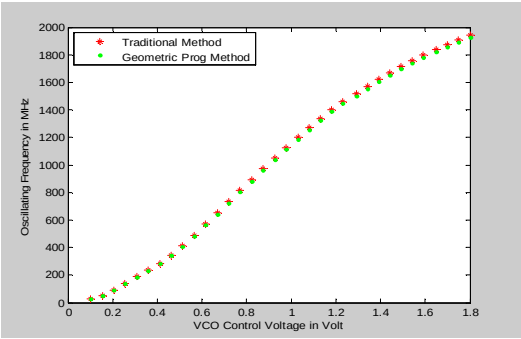

Fig.5.Control voltage versus oscillating frequency characteristics of current starved VCO circuit

Table 3

Performance comparison of CSVCO using both traditional and geometric programming method

Factor	CSVCO using traditional method	CSVCO using geometric programming method
Frequency(f)	1.012GHz	1.0000457GHz
Frequency Deviation(Δf)	12MHz	45.7KHz
Power(P)	432.456µW	539.65µW
Phase Noise @1MHz offset	-82.7 dBc/Hz	-82.6 dBc/Hz

VI. CONCLUSION

The centre frequency of oscillation of the VCO depends upon the sizing of the transistors. The frequency deviation from the desired value can be reduced by properly choosing the transistor sizes. By applying the convex optimization technique with frequency of oscillation as the main objective function we have minimized the frequency error.

In this paper we have applied the convex technique to find out the transistor sizing to meet only the desired frequency specification. The other constraints like area, power and phase noise can also be applied.

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