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AN ACCURATE ESTIMATION OF POWER USING VERILOG

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Abstract—**Power has become major design concern for complex VLSI circuits today. Designer needs tool(s) that accurately estimate the power dissipation for a given design. We need two categories of tools that are useful for this purpose. One is power optimization tools and, second is an analysis tool for estimating the power consumption in an existing netlist. This approach addresses the second issue by employing a VERILOG-based approach for analysis of power consumption in CMOS logic designs. The design under test will either the result of logic synthesis with various optimization constraints or hand design done through schematic capture. The proposed approach used to analyse various benchmark circuits for power consumption, such as ISCAS bench mark circuits. The presented approach in this paper consists of three phases: (1) Designing smart VERILOG simulation models, (2) Measuring transition activity at each node of the netlist and then estimate the power based on this activity and on fan out at each node, (3) Generation of smart input stimuli that achieve an upper bound in transition activity and hence power consumption. The estimates produced by this approach may provide useful feedback to designers or synthesis tools, allowing for better exploration of the design space.**

***Keywords*—Leakage power, Dynamic power, power dissipation, Bench mark, Verilog.**

I. INTRODUCTION

The scaling of CMOS devices in the present technology generation results in higher integration density and hence improved performance of VLSI circuits. However, this trend of scaling also indicates in significant increase in power dissipation. We should estimate an accurate leakage and dynamic power [1], [2]. It has been reported that the leakage power has become significant portion of the total power [5], and it is expected to even dominate the dynamic power in near future. Thus, developing an efficient technique for an accurate estimation of power dissipation has become more important for designing VLSI circuits.

Efficient power estimation CAD tools are increasingly becoming a necessity for today's technology. Synopsys switching activity format (SAIF) provides an accurate method to profile the state-dependent (SD) leakage power and path-dependent (PD) dynamic power [6]. This method requires that the technology libraries be already characterized for their leakage power by the vendor and it lacks the necessary flexibility and adaptability to obtain more user-specific data from the netlist.

In this paper, we have presented a VERILOG-based power estimation technique, which can be used in a standard cell based design flow to profile both state-dependent leakage power dissipation of a gate level design as well as its path-dependent dynamic power dissipation. The VERILOG language is used in many simulation and synthesis tools at the front end of the design flow. We have applied the proposed technique to some bench mark circuits synthesized by 65 nm library using Synopsys Design Compiler.

The rest of the paper is organized as follows: In section (2), we provide an overall flow of the proposed technique. In section (3), the characterization process of the technology library cells are discussed. In section (4), we present power model. In section (5), we present experimental results using some bench mark circuits. In section (6), we draw some conclusions.

II. VERILOG-BASED POWER ESTIMATION METHODOLOGY

VERILOG can be used in an integrated environment of the design, simulation and power estimation, by employing appropriate gate models. In this methodology, as shown in Fig.1, we have used power models of gates that allow tracing the probability of static levels of the signals at the input ports as well as the signal transitions at the output ports.

The synthesis tool provides optimized gate level netlist of the design, which can be obtained in Verilog format. The components present in the netlist are primitive gates such as INV, AND, NAND and NOR gates. A test bench is required to apply the test vectors set to the top level design and evaluate the power estimation of the circuit. Finally, a Verilog simulator is used to evaluate an accurate state dependent and path dependent (SDPD) power dissipation of the design.

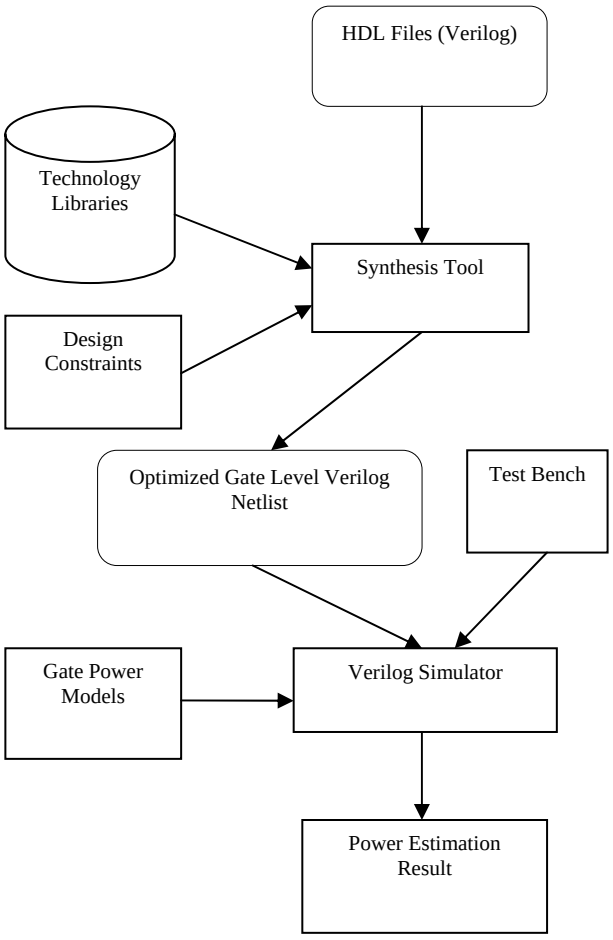

Fig.1 VERILOG-based power estimation flow.

III. CHARACTERIZATION OF LIBRARY CELLS

In order to accurately estimate the leakage power of a large gate level netlist for a particular input pattern, we need to annotate the gate's model with their state dependent leakage power and path dependent dynamic power. We employed gate models of 65 nm technology in this approach. The leakage power and dynamic power of all the standard cells are logged to look up tables which are incorporated in the gate power model. Based on the power models of the primitive gates the simulator produces the power.

The leakage power of 2 input NAND gate for typical and fast corners of the process is shown in tableI.

TABLEI
LEAKAGE POWER FOR 2 INPUT NAND GATE

NAND gate	Typical corner	Fast corner
	Leakage Power (nW)	Leakage Power (nW)
	C	C
00	2.281	5.187
01	4.029	23.076
10	2.185	12.360
11	7.713	50.897

IV. POWER MODEL

To find out the appropriate relationship between the logical behavior of a CMOS circuit and the power it can dissipate, the following assumption [1] are made:
(1). the only capacitance in a CMOS gate is at the output node.
(2). Current is either flowing from Vdd to the output capacitor (a 0-to-1 transition) or it is flowing from the capacitor to ground (a 1-0to-0 transition).
Based on these assumptions, it can be proven that energy dissipated by a CMOS gate is given by

$$P = NC (Vdd)$$

Where C is the output load (directly related to the gate fan out) and N is the total number of transitions (low to high or high to low) at the output of the gate. By monitoring the switching activity at each node in the network and applying the above equation, a reasonable assessment of the power consumed by a certain circuit can be found. In addition, it is apparent from the equation that by maximizing the transition activity, designers can study worst case power dissipation scenarios and possibly restructure the logic to optimize for heat dissipation.

This paper discusses a VERILOG based power estimation environment. VERILOG modeling techniques were used to design smart gate models that maintain records of their transition activity. Additionally, smart input stimuli that tend to maximize the switching activity were applied to the different circuits with the purpose of yielding an upper bound on power consumption.

V. SIMULATION RESULTS

The efficacy of the proposed technique for dynamic and leakage power estimation has been evaluated by the simulation of 10, ISCAS bench mark circuits. All circuits were synthesized with a 65 nm technology library using Synopsys Design Compiler. The output netlist contains only INV, NAND and NOR gates with up to four inputs and was saved in VERILOG format. A test bench was developed to configure the instantiated top-most design and to apply 100 random input vectors to the bench mark. The results of leakage and dynamic power estimation for the bench mark circuits for typical and fast corners of the process at high and low temperature are shown in table II. The data presented in table II also reveals that leakage power can extremely vary with different operating conditions. We also performed the logical simulation of all benchmark circuits using VCS tool to verify the functioning of the circuits. The figures Fig.2, 3, 4 and 5 show the logical simulation results.

VI. CONCLUSION

we have presented a VERILOG–based technique for dynamic and leakage power estimation of gate level net lists. Integrating simulation and power estimation into an

environment is useful for an improved utilization of VERILOG for the power critical deep-submicron VLSI systems design. In this approach, we have employed power models of cells which trace the state probability as well as the transition probability of the signals in the course of a simulation. These data are later used to accurately estimate the state-dependent leakage and path dependent dynamic power dissipation of the design. The results also show that the leakage power contribution to the total power dissipation is not significant for this particular 65 nm technology. Therefore, the high accuracy offered by the proposed technique is more desirable for more advanced technologies.

TABLE II
POWER ESTIMATION RESULTS FOR BENCHMARK

circuit	Typical corner		Fast corner	
	:C		C	
	Leakage power (nW)	Dynamic power (µW)	Leakage power (nW)	Dynamic power (µW)
74181	341.23	48.93	1919.80	14.05
74182	59.60	1.95	345.81	9.63
74283	258.74	8.26	3609.50	10.76
74L85	637.09	8.26	3609.50	10.76

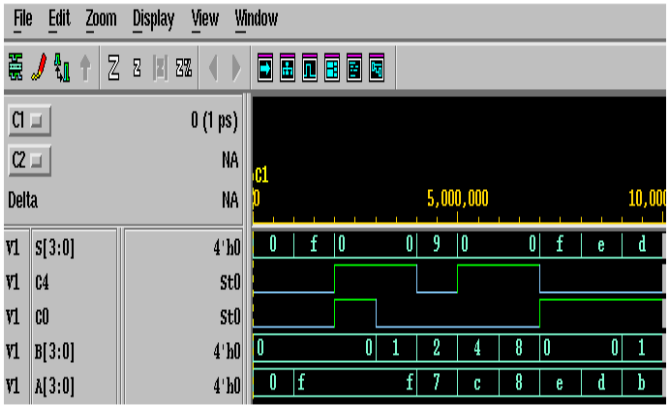

Fig.2 Logical simulation result for 74283 circuit

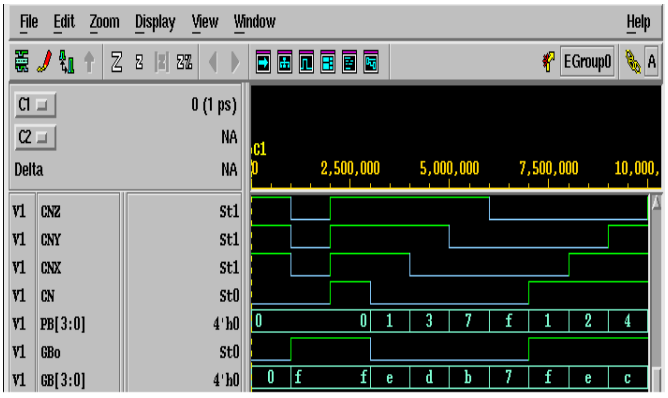

Fig.3 Logical simulation result for 74182 circuit

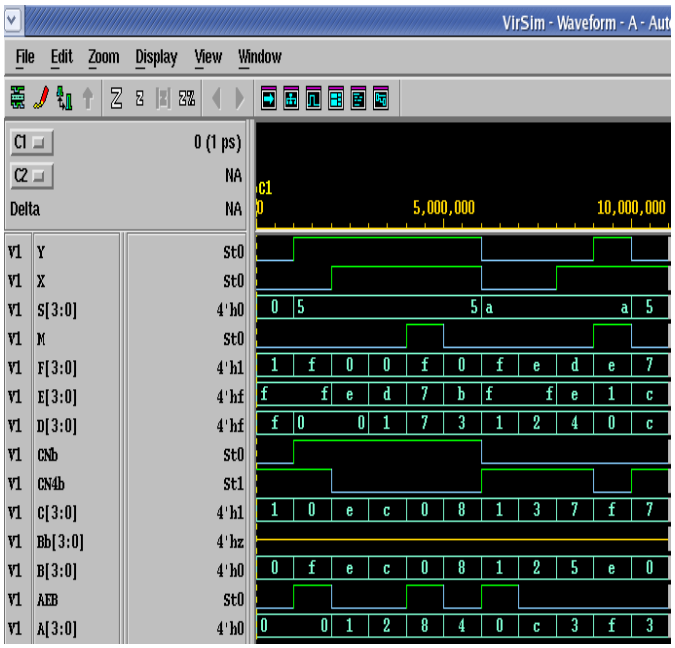

Fig.4 Logical simulation result for 74181 circuit

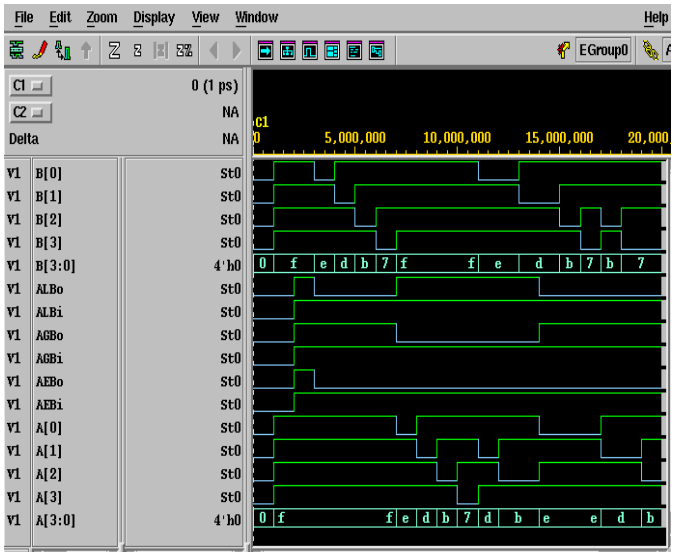

Fig.5 Logical simulation result for 74L85 circuit

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