Analysis and Design of a 1GHz PLL for Fast Phase and Frequency Acquisition

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***Abstract*—Phase locked loops find wide application in several modern applications mostly in advance communication and instrumentation systems. PLL being a mixed signal circuit involves design challenge at high frequency. This work analyses the design of a mixed signal phase locked loop for faster phase and frequency locking. The PLL is designed in GPDK090 library of CMOS 90nm process to operate at a frequency of 1GHz with a lock time of 280.6ns. This PLL circuit is observed to consume a power of 11.9mW from a 1.8-V DC supply.**

***Keywords*—Phase frequency detector (PFD), loop filter, voltage controlled oscillator (VCO), phase-locked loops (PLLs).**

I.INTRODUCTION

The most versatile application of the phase locked loops (PLL)[1] is for clock generation and clock recovery in microprocessor, networking, parallel and serial data communication, and frequency synthesizers. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Many present communication systems operate in the GHz frequency range. Hence there is a necessity of a mixed signal PLL [1] which must operate in the GHz range with less lock time. The PLL performance depends upon its order. If 'n' is the order of loop filter than 'n+1' is the order PLL [2]. The stability of the whole PLL system depends on the order of the loop filter. The voltage controlled oscillator (VCO) is the heart of the PLL. The present work focuses on the redesign of a PLL system using the 90nm technology. Hence a current starved ring oscillator has been considered for its superior performance in form of its low chip area, low power consumption and wide tunable frequency range. The PFD described in [4] has been considered for its fast acquisition capability. The result of extensive simulation is reported here. The remaining part of the paper is organized as follows. Section II describes the general architecture of a PLL system. In section III the design and synthesis environment has been outlined. The results of simulation study are discussed in section IV. Finally the finding of the study has been concluded in section V.

II. ARCHITECTURE OF PHASE LOCKED LOOP

Phase locked loop is a feedback system that compares and locks the phase and frequency of an input signal with respect to the available reference signal. The comparison is generally performed by a phase and frequency comparator which is technically known as phase frequency detector (PFD). The output of the PFD is fed to a charge pump circuit to get a constant current at the output. The charge pump output is passed through a low pass filter to generate the control voltage for the VCO circuit. Hence there are five functional blocks in a PLL circuit such as phase frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO) and frequency divider. The frequency divider is an optional block. It may or may not be included in the circuit diagram. Most of the practical design a buffer circuit is added to the output of the VCO. The PLL architecture having all the above building blocks including the buffer is shown in the Fig.1. The details of all the blocks are explained in the following sections.

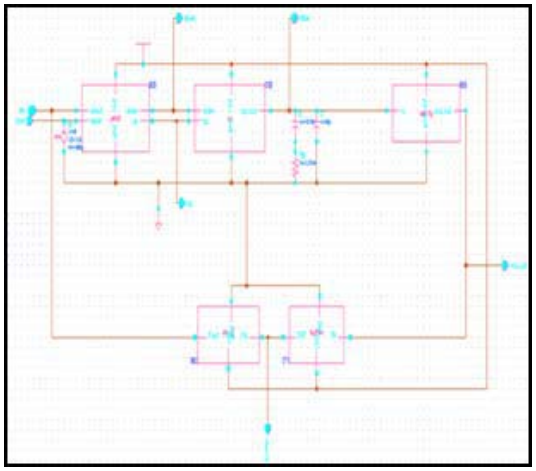

Fig.1.Block Diagram of a PLL System

A. phase frequency detector

The PFD circuit is used to find the difference in phase and frequency between the two input signals reference frequency (F_{ref}) and input frequency (F_{in}) which is fed back from the output of the VCO. The PFD generates two output signals UP and DOWN that switches the output current of the pump.PFD

circuit is generally implemented using D flip flops (DFFs) [1],[3].The output of the PFD depends upon both phase and frequency of the input signals. Initially both the signals will be low. When one of the PFD input rises the corresponding output becomes high. A pass transistor DFF based PFD architecture as in [4] is used in this PLL design. The simulation waveforms of PFD when Fref leads Fin are shown in the Fig.2.

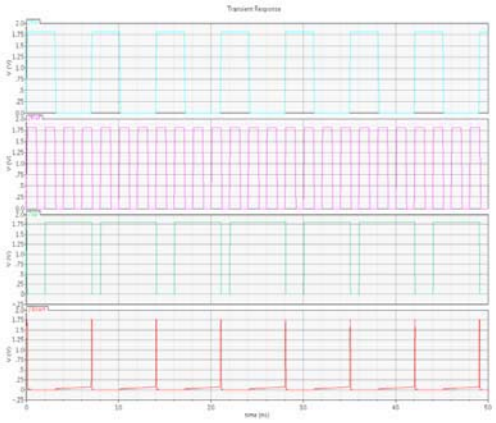

Fig.2.PFD behavior when F_{ref} Leads F_{in}

B. charge pump and loop filter

Charge pump circuit is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. Charge pump circuit gives a constant current of value I_{PDI}. The amplitude of the current always remains same but the polarity changes which depend on the value of the UP and DOWN signal. The schematic diagram of the charge pump circuit is shown in the Fig.3.When the UP signal goes high M2 transistor turns ON while M1 is OFF and the output current is I_{PDI} with a positive polarity. When the down signal becomes high M1 transistor turns ON while M2 is OFF and the output current is I_{PDI} with a negative polarity.

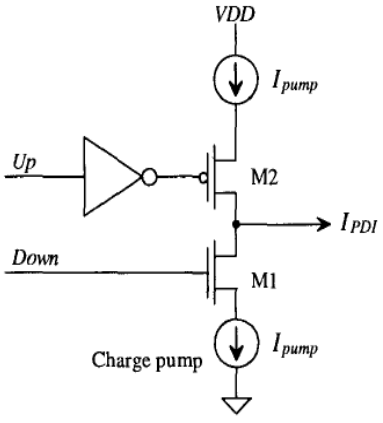

Fig.3.Schematic Diagram of Charge Pump Circuit [3]

The charge pump output current [3] is given by

$$I_{PDI} = K_{PDI} \times \boldsymbol{\Delta\Phi} \quad (1)$$

Where $K_{PDI} = \frac{I_{pump}}{2\pi}$ (amps/radian) (2)

$$\Delta\Phi = \Phi_{in} - \Phi_{ref} \quad (3)$$

The phase difference ΔΦ is zero when loop is in lock.
The VCO input voltage is given by

$$V_{invco} = K_f \times I_{PDI} \quad (4)$$

The passive low pass loop filter is used to convert back the charge pump current into the voltage. The output voltage of the loop filter controls the oscillation frequency of the VCO. The loop filter voltage will increase if F_{ref} leads F_{in} and will decrease if F_{in} leads F_{ref}. If the PLL is in locked state it maintains a constant value. The simulation result for loop filter with PFD when F_{ref} Leads F_{in} is shown in the Fig.4.

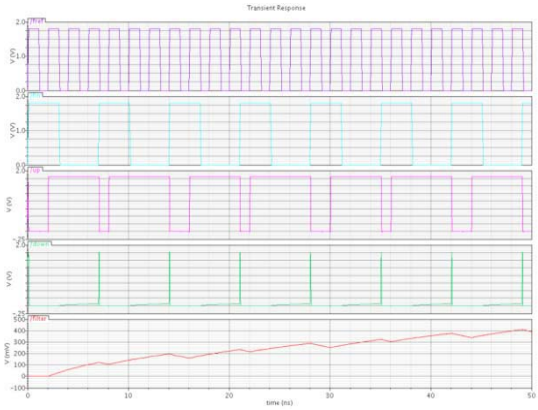

Fig.4.Simulation Result for Loop Filter with PFD When F_{ref} Leads F_{in}

C. voltage controlled oscillator

The popular current starved ring oscillator is used as VCO in this study. Here the number of inverter stages is fixed with five. The schematic of the VCO is shown in the Fig.5.The center frequency of the VCO is 1GHz at 1.8V supply. The inverter stages are designed as mentioned in [3], [5].

Fig.5. Schematic of Five Stage Current Starved Ring Oscillator

VCO design parameters are listed in the Table I.

Table I
VCO design parameter

Parameter	Value
Center frequency	1GHz
No. of inverter stage	5
Inverter dealy	100ps
Load capacitance	65fF

The characteristics curve of the VCO is shown in the Fig.6.The gain of the VCO is given by

$$K_{vco} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \text{ (Hz/V)} \qquad (5)$$

In this design K_{vco} is 1.531 (GHz/V)

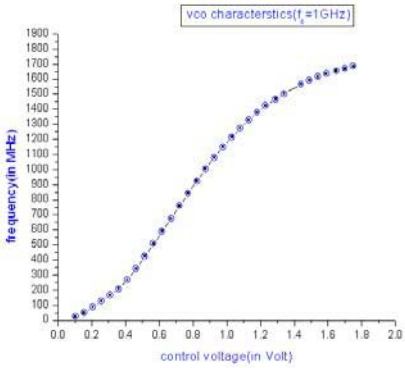

Fig.6.Characterstics Curve of VCO

D. frequency divider

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the VCO output signal. In this design a divide by 2 frequency divider is used. The output waveform of the divider is shown in the Fig.7.

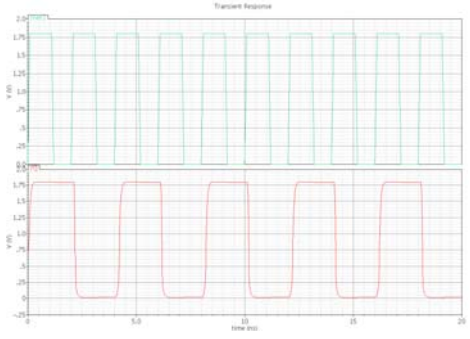

Fig.7.Simulation Result of Divide by 2 Circuits

III.SIMULATION ENVIRONMENT

The design entry of the circuits is carried out in the CADENCE Analog Virtuoso Environment using gpdk090 library. For performance analysis these circuits are simulated in the Spectre simulator of CADENCE tool. Different performance indices such that phase noise [6],[7], power consumption and lock time are measured in this environment. The phase noise which is a primary factor of concern in PLL design is defined as the noise power relative to the carrier contained in a 1Hz bandwidth centered at a certain offset from the carrier. Lock time of the PLL is defined as the time it takes to lock the PLL to a given tolerance. Transient, parametric sweep and phase noise analysis are carried out in this work to find out the characteristics of the circuits.

IV.RESULTS AND DISCUSSION

The control voltage and the phase noise simulation result of the PLL circuit are shown in the Fig.8 and Fig.9 respectively. From the Fig.8 it's clear that the PLL lock time is 280.6ns at 0.9V which is much better than the value as reported in [8]. The phase noise of the PLL is -54.12dBc/Hz. The design performance of the PLL is summarized in Table II.

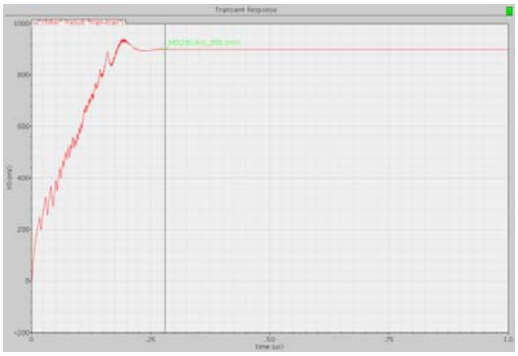

Fig.8.Transient behavior of VCO control voltage at loop filter output in GPDK090.

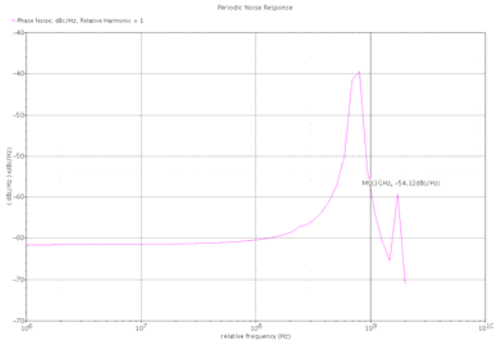

Fig.9.Phase Noise variation of PLL w.r.t. the operating frequency.

Table II
Summary of simulation

Parameter	Result of Current Work	Results reported in [8]
Technology	90nm	180nm
VDD	1.8V	5V
Lock Time	280.6ns	643.358ns
Frequency	1GHz	1GHz
Power Consumption	11.9mW	-
Phase Noise	-54.12dBc/Hz	-

V. CONCLUSION

In this paper we presented a PLL with a better lock time which is designed in CMOS 90nm technology using GPDK090 library. The lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the charge pump and loop filter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values we can achieve a better lock time. The simulation for the phase noise performance of the PLL is also carried out in this work.

REFERENCES

[1]. Roland E. Best, "Phase Locked Loops Design, Simulation and Applications," *McGraw-Hill Publication*, 5th Edition, 2003.

[2]. Dan H. Wolaver, "Phase Locked Loop Circuit Design," *Prentice Hall Publication*, 1991.

[3]. R.J.Baker, H.W.Li, and D.E.Boyce, "CMOS Circuit Design, Layout, and Simulation," *IEEE Press Series on Microelectronic Systems,* 2002.

[4]. M.Mansuri, D.Liu, and C.K.Yang, "Fast Frequency Acquisition Phase Frequency Detector for GSamples/s Phase Locked Loops," *IEEE Journal of Solid State Circuit, Vo*l. 37, No. 10, Oct., 2002.

[5]. S.M.Kang, and Y.Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design," *McGraw-Hill Publication*, 3rd Edition, 2003.

[6]. A.Mehrotra," Noise Analysis of Phase-Locked Loops", *IEEE Tran. On Circuits and Systems-I: Fundamental Theory and Applications,* VOL. 49, NO. 9, SEPTEMBER 2002.

[7]. Alper Demir," Computing Timing Jitter From Phase Noise Spectra for Oscillators and Phase-Locked Loops with White and 1/f Noise*", IEEE Tran. On Circuits and Systems-I: Regular Papers,* VOL. 53, NO. 9, SEPTEMBER 2006.

[8]. H.Janardhan, and M.F.Wagdy "Design of a 1GHz Digital PLL Using 0.18µm CMOS Technology," *IEEE Proc. Of the Third International Conference on Information Technology*, 2006.